Process Development of a Novel Pseudo Two-Phase CCD Pixel Using Transparent Conducting Oxide Electrodes

By

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Abstract

A microelectronic fabrication process for an all-transparent electrode, pseudo two-phase CCD image sensor pixel, resistant to DC shorting and compatible with a self-aligned barrier implant, was proposed, boasting the advantage of simple and cost-effective fabrication combined with high responsivity over the entire wavelength spectrum of visible light. The feasibility of such a process was proven by fabricating, testing, and analyzing a DC version of the device structure. Work entailed individual process design and development, integration of unit processes into a manufacturing flow, fabrication, testing, and failure analysis. Countermeasures to high-frequency failure modes were implemented as part of the second-generation design. Prototype devices were fabricated and tested for DC yield on 150 mm silicon wafers using standard semiconductor processing steps exclusively at Eastman Kodak Company in the Image Sensor Solutions B81S Microelectronic Fabrication Facility.

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Chapter 1

Introduction

Solid-state charge-coupled device (CCD) image sensors are comprised of integrated circuits that use photogates and/or photodiodes to generate an electrical signal that is proportional to the intensity of incident illumination. Design variations have been developed to create color, as well as black and white, imagers. Regardless of the architecture, the charge generated in each pixel must be transported by line and column shift registers into an output circuit. It is essential that this charge transfer occur with a minimum of loss.

A CCD is, in essence, a string of adjacent MOS capacitors built in p-type silicon biased into deep depletion, forming a "potential well" under each electrode. The depth of the depletion regions (or potential wells), may be controlled by varying the bias voltage, the gate dielectric thickness, the work function of the gate electrode, or the doping in the semiconductor itself, as illustrated in Figure 1.

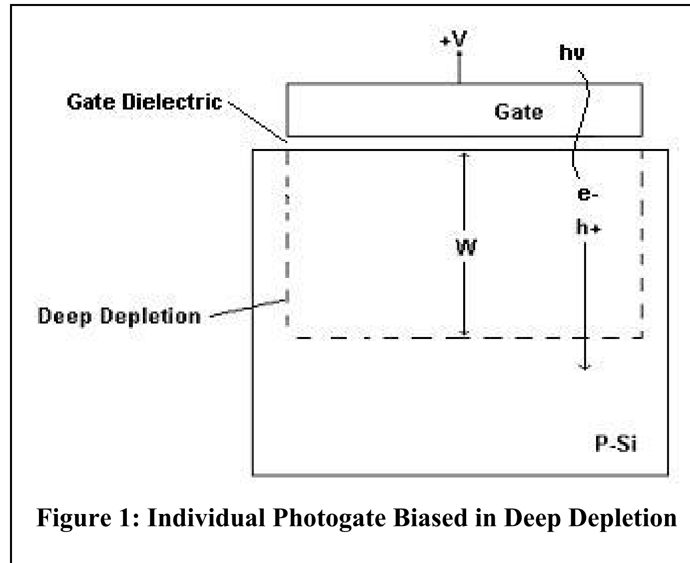

Figure 1: Individual Photogate Biased in Deep Depletion

Figure 2 illustrates a full-frame devices, in which light absorbed in the substrate under the gate electrode generates electron-hole pairs. If Gate 1 is biased into deep depletion, the holes are swept into the substrate, while the electrons are captured in the potential well, forming a "charge packet," as shown in Figure 2b. Biasing of gate 2 allows the charge to be shared between the two gates, as illustrated in Figure 2c and d. Reduction of the bias on the first gate results in the charge flowing solely into the potential well under gate 2, (Figure 2e and f). This sequence illustrates the basic charge transport mechanism of a CCD [1]. Care must be taken in design and fabrication of devices to insure that the depletion regions of adjacent electrodes overlap to facilitate complete and efficient transfer of charge.

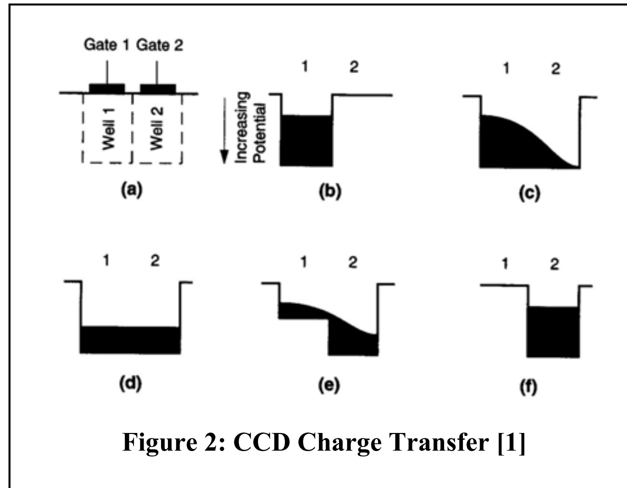

Figure 2: CCD Charge Transfer [1]

Captured charge packets are then transferred in a parallel manner, line-by-line, into a serial shift register. From here, the charge packets enter an amplifier circuit in the periphery of the imager for transfer to off-chip signal processing electronics. Figure 3 illustrates the basic full frame device architecture. In this design, a CCD can be used both for image capture and charge transport across the chip. In interline transfer devices, the image is captured in a separate photodiode instead of under the gate electrode, although the charge transport mechanism is the same.

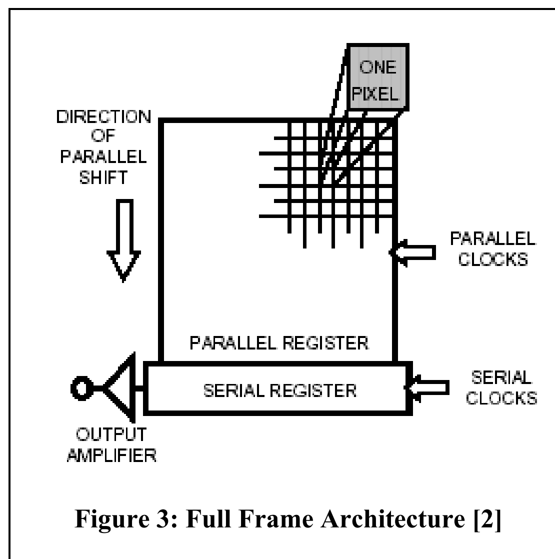

Figure 3: Full Frame Architecture [2]

A number of system architectures are available to facilitate charge transport, each with their respective strengths and weaknesses. Conceptually, one of the simplest of these architectures, the four-phase clocking system, boasts a very simple fabrication process and a high charge capacity in each pixel at the cost of a complex clocking scheme. Four gates are required per pixel, and charge transfer can be bi-directional. Three-phase architecture reduces the number of gates per pixel to three, and charge transfer is still bi-directional. The major drawback of the three-phase architecture is that the charge capacity of each pixel is significantly reduced. Fabrication complexity is similar to that of the four-phase device. A two-phase clocking system simplifies required clock signal generation significantly, and charge capacity is typically improved over that of the three-phase device, although not to the capacity exhibited by four-phase devices.

Numerous varieties of two-phase architectures are available. A basic implementation, known as pseudo two-phase, is shown in Figure 4. The doping of the semiconductor under every other gate region is adjusted, typically by ion implantation, in order to create a "staggered" well region, often times referred to as a barrier region, which causes collected charge to shift in the direction of the widest (deepest) depletion region in the well. In this way, only two clock signals are required for charge transport. The major drawbacks of this architecture are fabrication complexity is increased, charge can only be transferred in one direction, and four gates are required per pixel.

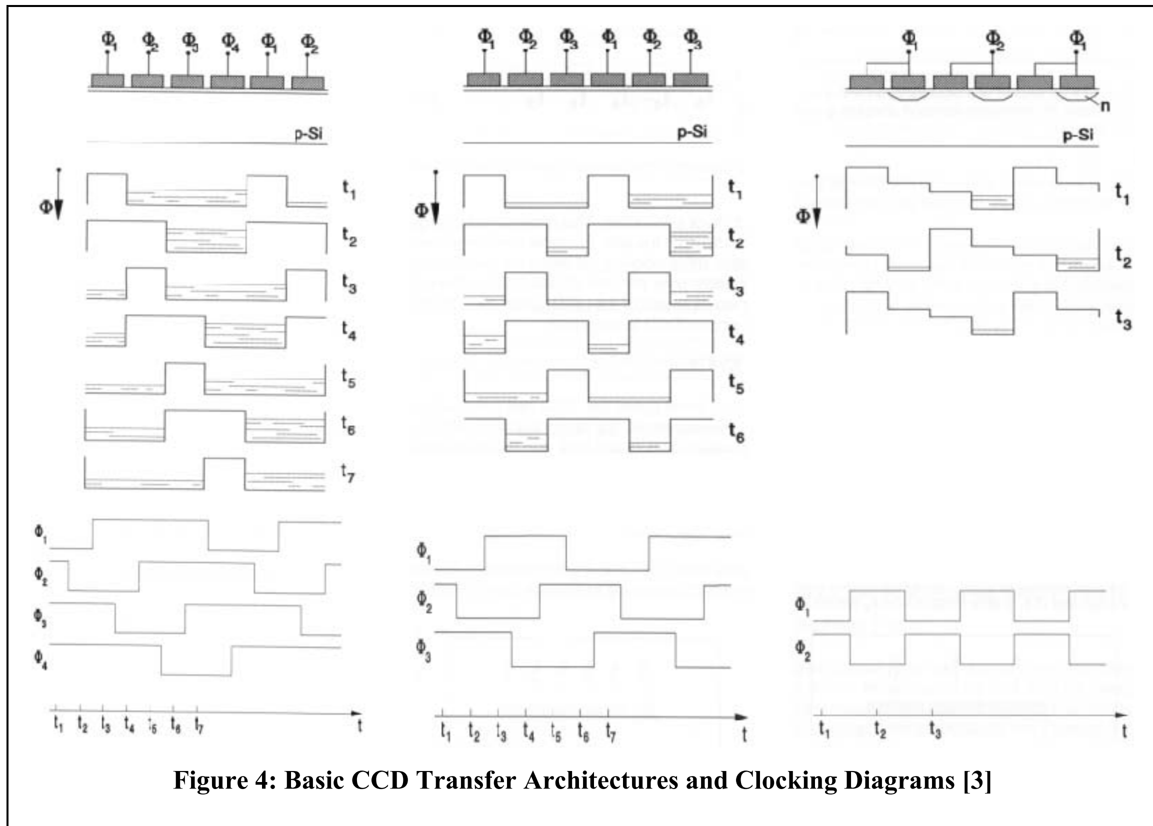

Figure 4: Basic CCD Transfer Architectures and Clocking Diagrams [3]

Although the CCD was invented at Bell Labs by W. Boyle and G. Smith in 1970 [4,5], it wasn't until the wide-scale entry of camcorders into the consumer market that CCDs began to take hold as the premier image sensor for mass market electronic imaging applications [6]. Since that time, technology trends have shown a continued increase in pixel count per imager for higher resolution. This results in a continuous pixel-size shrink, resulting in a reduction in the light-sensitive area in each pixel. As the light-sensitive area of each pixel shrinks, the overall responsivity (ratio of the output signal to the incident input signal [7]) of each pixel is reduced. In order to offset this loss, sensor manufacturers struggle to improve the responsivity per unit area of the sensor and maximize the fill factor, or useful sensitive area, of each pixel. A number of processing variations are employed commercially, addressing these issues in various ways.

Commercial CCD image sensors typically use highly doped polycrystalline silicon (poly-Si) as an electrode material due to its compatibility with standard semiconductor manufacturing processes, conductivity, and transmission properties. However, doped poly-Si has been shown to suffer from excessive light absorption, especially in the blue region of the spectrum. This is undesirable because it makes the efficiency of the sensor a function of incident wavelength. Backside thinning of full-frame imagers allows incident light to illuminate the sensor from "behind," reducing absorption by the electrode structures [8]. As the light-sensitive region of the backside-thinned device and the CCD transfer structure are the same, high quantum efficiency (the number of signal electrons created per incident photon of light at a given wavelength [7]) is achieved, but at exceedingly high manufacturing complexity and cost. Alternatively, the addition of micro-lenses to the device surface focuses incoming light into high responsivity regions [9]. This approach suffers the effect of responsivity roll-off at the edges of the device because of the effects of large angles of incidence, along with substantially increased manufacturing complexity and device cost.

Other novel approaches, such as the "virtual phase" device, in which electrodes are not used over barrier regions [10], and the "light window" approach, in which gate structures are modified to allow direct access to incoming light [11,12], all have "the undesirable effect of increasing the manufacturing process complexity and/or compromising other sensor performance parameters [13]," and therefore have not been commercially adopted.

Approaches using a transparent conducting oxide (TCO) for one electrode have been proposed in several forms [14,15]. These approaches, successfully commercialized

by Eastman Kodak Company in 1999 [16], reduce the unwanted absorption by replacing a poly-Si electrode for one phase of a two-phase device with indium-tin oxide (ITO).

Indium Tin Oxide (ITO) is a highly degenerate n-type wide band gap semiconductor [17]. It is finding wide acceptance as a transparent conductor (TC) in a variety of opto-electronic applications, such as solar cells, flat panel displays, flexible electro-optical devices [18], electrochromic devices (smart windows), transparent gate gallium arsenide MESFETs [19], and high-quantum efficiency charge-coupled devices (CCD) [25], and charge injection device (CID) image sensors [20] due to its high transmittance and low resistivity, reported as high as 95% and as low as 1E-4 Ω·cm, respectively [21].

Figure 5 provides a relative comparison of quantum efficiency as a function of wavelength for poly-Si, ITO, and ITO with a micro-lens. This approach, however, still leaves some unwanted blue absorption due to the remaining poly-Si phase. Going one step further, an all-TCO-electrode device would alleviate the problem of unwanted blue absorption, while retaining highly efficient charge transfer by using self-aligned barrier implants, but at the cost of substantial manufacturing complexity [22,23].

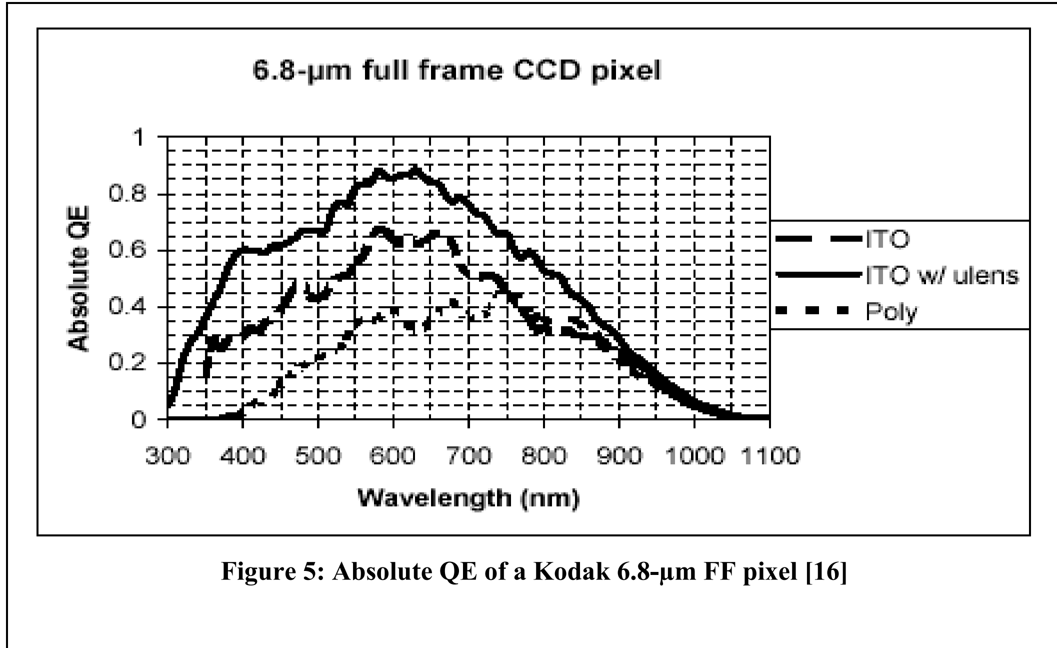

Figure 5: Absolute QE of a Kodak 6.8-µm FF pixel [16]

Clearly, opportunities exist for improving solid-state image sensors by maintaining performance during feature shrink, improving transmission properties of the component materials, and developing fabrication processes compatible with CMOS manufacturing. This work summarizes preliminary studies of a novel approach to fabricating an all-transparent-electrode pseudo two-phase CCD [24], using ITO as the electrode material.

Chapter 2 will review key performance issues and specifications of CCD operation. The proposed all-transparent-gate process is introduced and critical processing issues stated. Chapter 3 will summarize experimental equipment, conditions, and studies conducted to complete this work. Chapter 4 will present and discuss the results of these experiments. Chapter 5 will present conclusions of this work and recommendations for future study.

Chapter 2

CCDs: Historical Development and Proposed Device

2.1 CCD Evolution

Transparent gate CCD imagers for high quantum efficiency, first described in early 1978 by Thompson et al., were embodied in a four-phase time-delay-and-integration (TDI) device [25]. Pixels were 76 μm on a side. Working devices were fabricated and characterized with reasonable results, although the complex clocking required for four-phase devices limited this technology to specialized high-end imaging applications.

A virtual-phase device using transparent gates of tin oxide (TO) was first described by Keenan and Harrison in 1985 [26]. Utilizing only a single TO electrode, a working 420 x 420 array of 40 x 40 μm pixels was fabricated and tested to demonstrate the improvement in responsivity compared to a poly-Si gate device. Although clocking becomes much simpler in the virtual phase embodiment, charge capacity is limited without the use of excessive clock voltages, again restricting the usefulness of this device in mass-market image sensing applications.

The definitive work utilizing transparent gate electrodes for mass-market full-frame CCD imagers was reported by Kosman et al. in 1990. A 1280 x 1024 array of 16 x 16 μm pixels using a two-phase architecture with one poly-Si and one ITO electrode was

described [15]. A 38% responsivity improvement was observed across the visible spectrum compared to an all-polysilicon device [27]. This set the stage for the 1999 commercialization of the Kodak Blue Plus color image sensor line of full-frame, two-phase CCD image sensors utilizing a single ITO electrode.

In December of 1990, Christianus Hermaneus Leopold Weijtens published his doctoral thesis on “Indium Tin Oxide for Solid-State Image Sensors” as part of his work at Philips Research Laboratories [28]. This report detailed the integration of indium tin oxide in place of poly-Si for half of the electrodes in a frame-transfer imager, including, but not limited to, deposition and characterization of ITO films; integration of ITO with standard IC processing equipment and methods; and characterization of working devices. To date, however, no comprehensive documentation describing a full TCO device is available in the literature.

Two-phase CCDs are preferable for digital still camera applications because of the simplicity of required clocking schemes. Only two clock signals are required to operate the device, while overlap and lag of the two signals is not critical to device operation [29]. The preferred embodiment of the device uses a pseudo two-phase design, requiring ion implants under every other electrode in order to engineer the potential wells wells, resulting in the charge shifting in a single direction, as depicted in Figure 6 [30].

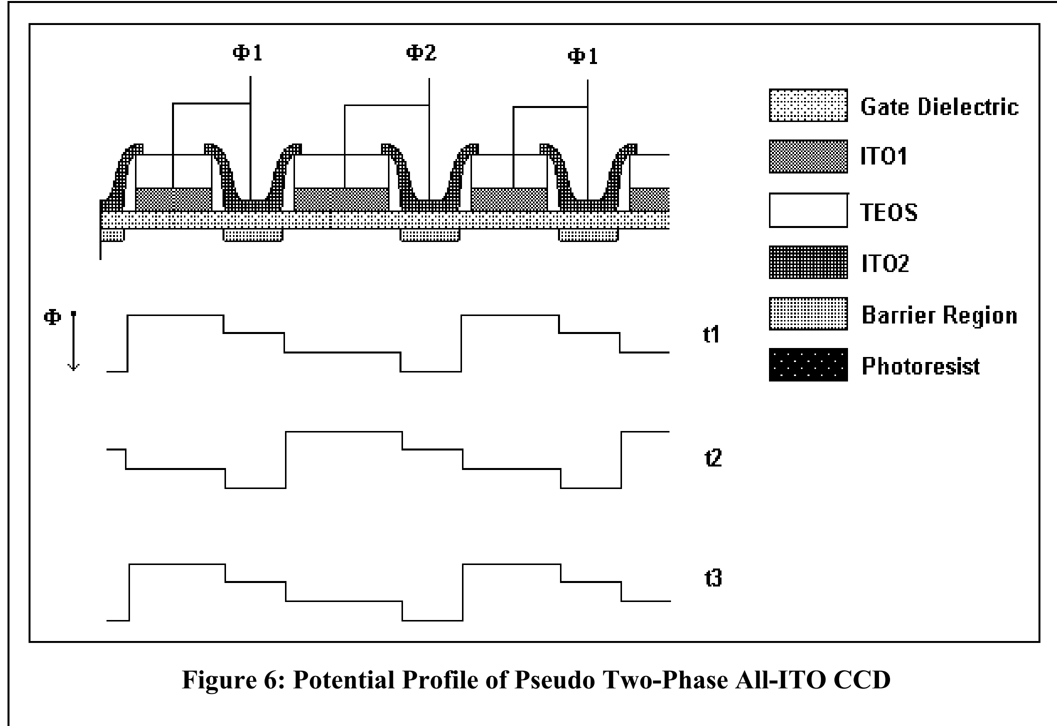

Figure 6: Potential Profile of Pseudo Two-Phase All-ITO CCD

2.2 Proposed Fabrication Process

Fabrication of a full TCO device is based on a simple manufacturing process using oxide-nitride-oxide (ONO) gates under the ITO electrodes. The first-level ITO layer is deposited and patterned using standard lithographic processes [24]. A sidewall spacer is formed around the first-level ITO electrode for electrical insulation. The second-level ITO film is deposited, patterned, and the device continues along standard semiconductor process flows.

Breaking the entire process flow into modules, the wafers begin at the active level, where the gate oxide is thermally grown, followed by low-pressure chemical vapor deposition (LPCVD) of a silicon nitride layer, which will act as a diffusion barrier in the gate dielectric stack. The wafer is photo-lithographically patterned, using standard processing techniques, and the LPCVD nitride film is removed from regions not

protected by photoresist using reactive-ion etch (RIE) techniques in a fluorocarbon plasma. The photoresist is removed from the device and the wafers are subjected to a thermal field oxidation. The unetched nitride serves as a diffusion barrier during the field oxidation, allowing field oxide growth in the unprotected regions, while nitride oxidizes approximately two orders of magnitude more slowly than the silicon, forming the top oxide of the ONO gate dielectric stack. The result is a wafer very similar to a CMOS wafer having LOCOS isolation, except the ONO stack on our wafer will remain as part of the device.

The formation of the first-level electrode ensues, beginning with deposition of a TCO. Deposition of the ITO was accomplished by sputtering, which is common in the industry [31]. The ITO was covered with a film of tetra-ethyl-ortho-silicate (TEOS) oxide by plasma-enhanced chemical vapor deposition (PECVD) and sent back for photo-lithographic patterning of the first-level electrode. Figure 7a shows a cross-section of the pixel region of the imager at this step.

With the first-level electrode pattern defined by the photoresist, a plasma etch is used to remove the oxide. A second plasma etch, utilizing a methane/hydrogen gas mixture [32], is used to etch the ITO selectively to the photoresist and underlying dielectric. The resist is removed and the wafers are cleaned, as shown in Figure 7b.

The spacer formation commences with a second TEOS PECVD film being deposited conformally across the wafer as shown in Figure 7c. This is followed by an anisotropic RIE etch in a fluorocarbon plasma, resulting in the formation of a sidewall spacer, leaving the first-level electrode totally surrounded by oxide. A PECVD oxide was chosen for the spacer over silicon nitride due to the tendency of ITO films to reduce

to metallic indium or metallic tin in the presence of hydrogen plasmas (as is common in the deposition of nitride). This reaction reduces transparency of the film and results in degradation of device performance [33].

Following spacer formation, ion implantation of the barrier region is undertaken, self-aligned to the edges of the spacers and directly under what will become the second-level electrode region. Figure 7d illustrates our device with the barrier region formed.

Finally, the formation of the second-level ITO electrode is accomplished in a manner similar to that of the first. The ITO is sputtered across the wafer, patterned lithographically, and etched selectively to oxide. Following resist ash and clean, the resulting device appears as shown in Figure 7e. This completes the formation of the CCD itself.

The formation of pads for electric test would begin with a thick TEOS oxide deposition across the entire wafer for protection and isolation, followed by a thermal anneal to activate dopants and densify the PECVD layers. Contact lithography is performed, and the TEOS oxide is etched in another fluorocarbon plasma to open contacts to the ITO electrodes. Following resist ash and clean, the wafers are sent on for metallization. Metallization begins with a brief buffered oxide etch (BOE) dip to remove any remaining oxide films in the contact areas, quickly followed by deposition of the level 1 metallization. First, a conductive barrier layer of TiW is deposited, followed by an Al/Si film. The metal is photo-lithographically patterned and etched. Following resist ash and clean, device formation is complete, and the wafers are ready for electrical test. Full SUPREM-4 Modeling flows are available in Appendix A: SUPREM-4 Modeling.

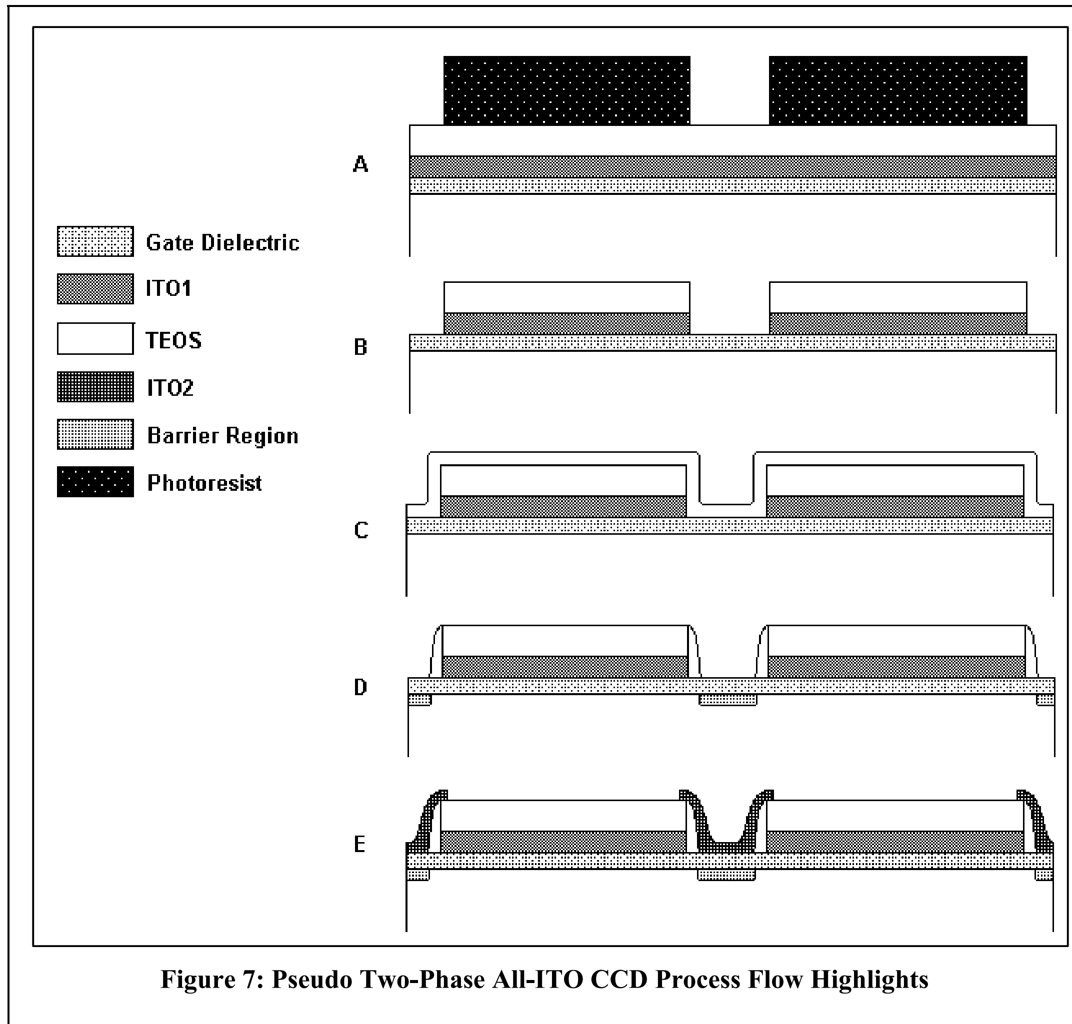

Figure 7: Pseudo Two-Phase All-ITO CCD Process Flow Highlights

As straight forward as the above process flow appears, successful implementation first required development of several unit processes that addressed critical yield issues. For example, deposition of the ITO films required reduction in the number of particles produced by the sputter process, and spacer formation required minimizing damage to the gate dielectric and repair of any gate dielectric damage encountered during processing. Chapter 3 discusses the equipment, experiments, and analysis used to resulve these issues and implement this process.

Chapter 3

Experimental Equipment and Studies

The strategy adopted was to first develop the required individual unit processes required for the devices, including low-particle deposition of the transparent conducting oxide, a hard-mask etch process, an etch for the first-level TCO electrode, the spacer formation process, and a thin PECVD oxide "reformation." Following individual process development, first-generation devices were fabricated. After failure mechanisms were identified, unit processes and the integrated process flow were refined prior to fabrication and testing of second-generation devices.

Data was obtained throughout the fabrication sequence from three primary sources: standard in-process metrology, scanning electron micrographs of vertical cross sections at various key steps in the manufacturing process, and post-fabrication DC test and failure analysis data. In-process metrology consisted of spectroscopic ellipsometry film thickness measurements from a KLA-Tencor UV1280SE system on product and monitor wafers included at appropriate processing stages, particle scans on product and monitor wafers from a KLA-Tencor Surfscan 6220 and a KLA-Tencor AIT 7600, and standard inspections using optical microscopy. Scanning electron micrographs of wafers at various points in the process, although destructive, were used for basic process characterization and identification of areas for improvement. The micrographs were

obtained by cleaving the samples and imaging in a Hitachi S-6200H SEM using magnifications in a range of 25,000 to 150,000X. Post-fabrication DC testing was completed using standard CCD automated test systems.

Particle reduction in the ITO deposition required defect characterization data involving Energy Dispersive X-Ray Spectroscopy (EDS) compositional analysis and SEM micrographs, in addition to standard defect density data. Both thin film deposition and etch involved designed experiments to optimize details and processing parameters. Each study is now discussed in detail.

3.1 ITO Deposition

Deposition of ITO has been reported from a variety of methods, including, but not limited to, chemical vapor deposition, spray pyrolysis, vacuum evaporation, e-beam evaporation, and physical vapor deposition [37]. Control of film resistivity and visible-light transmission is of extremely high importance in the manufacturing of image sensors; therefore, the stoichiometry and crystal structure of the ITO film must be carefully controlled. Magnetron sputtering from an oxide target appears to be the preferred method for maximum compositional control without post-deposition treatments [36], combined with a minimum of induced film damage [37].

The sputtering system had a base pressure of 2E-6 Torr, achieved using a cryogenic vacuum pump. An ENI RPG-model pulsed bipolar DC power supply was used for deposition because it provided an asymmetric square wave, which disrupts the sputtering process and cleans off insulating areas of the target. This in turn reduces target arcing and, therefore, particle formation. The target was a water-cooled magnetron, hot-pressed powder (>98% density) of In_2O_3/SnO_2 in a 90/10% composition by weight.

Films for analysis were deposited to a standard thickness in an argon/oxygen ambient on 150 mm silicon wafers, which were covered with a 4000 Å thermal oxide film.

Manufacturing challenges in the fabrication of state-of-the-art ITO-electrode image sensors center around in-film defect reduction, as defects in ITO films have demonstrated a significant yield impact on area imagers [38]. Because of the nature of the proposed process, defects in deposited ITO films would likely have a high kill ratio due to shorting between the first-level and second-level electrodes. Therefore, deposition parameters were optimized to reduce defectivity.

The study first acquired a baseline of the current defect levels by mapping out defects on sample wafers with previously inscribed alignment marks using a KLA-Tencor Automated Inspection Tool (AIT). Particles were imaged in a scanning electron microscope (SEM) for shape and position. A focused ion beam (FIB) was used to obtain internal and cross-sectional images of defects of interest. Energy Dispersive X-Ray Spectroscopy (EDS) was used to assist in determining the composition of the particles. Results were used to propose an improved process.

3.2 Hard-Mask Etch

Etching of the first-level electrode first required development of an anisotropic etch of the TEOS masking layer, stopping on the ITO layer. Critical characteristics of the etch included complete clearing of the TEOS layer to avoid micro-masking and stringers of the first-level ITO, while avoiding sputtering of the underlying ITO layer onto sidewall surfaces, degrading pattern integrity.

In order to avoid sputtering of the ITO layer, a fluorocarbon etch with a moderate Argon carrier flow was developed on a Lam Research Corporation (LRC) Rainbow 4520

XL platform. Table 1 summarizes the etch parameters. Cross-sectional images from the SEM were used to evaluate sidewall profiles.

Parameter	Value
Pressure	60 mTorr
CHF3 Flow	40 sccm
C4F8 Flow	5 sccm
O2 Flow	10 sccm
Ar Flow	80 sccm
RF Upper Electrode	840 W
RF Bias Electrode	840 W
Gap Height	1.45 cm
Backside Helium Pressure	9 Torr
Etch Time	32 s

Table 1: Hard-Mask Etch Parameters

3.3 First-level ITO Etch

Dry etching of ITO was performed on a parallel plate RIE chamber. Etch time was optimized by using an optical emission spectroscopy (OES) system for optical endpoint detection and included a 25% overetch to account for etch non-uniformities and to remove any stringers.

Etch conditions were similar to standard ITO dry-etch parameters documented in the literature [32,39] and used a methane/hydrogen gas mixture in an argon carrier. This process, while etching ITO, deposits an amorphous carbon film on non-etching surfaces [40], providing near-infinite etch selectivity to oxide and photoresist. Cross-sectional SEMs were again used to evaluate results.

3.4 Spacer Etch

Unlike conventional CCDs using doped polysilicon electrodes, ITO electrodes do not oxidize to form an insulating sidewall. In order to insulate the electrodes, a sidewall-spacer technology was employed. Nitride spacers are not practical for ITO devices because of the tendency of ITO to reduce to a metallic sub-oxide in the presence of hydrogen at the temperatures and concentrations consistent with nitride deposition. Therefore, a TEOS layer was chosen as the sidewall-spacer material because of its compatibility with low-temperature processing in low-hydrogen environments, maintaining the integrity of the ITO.

Development of sidewall-spacer technology required conformal CVD TEOS deposition and an anisotropic oxide etch that was selective to the thin silicon nitride comprising the middle layer of the ONO stack. Further, the spacer surrounding the first-level electrode must be thick and dense enough to insulate the conducting layer from the second-level electrode, which is dependent not only on etch parameters but also on original spacer film deposition thickness [41]. However, too thick of a spacer will adversely affect charger transfer between pixels. A first-pass spacer module was designed with a screening experiment utilizing TEOS deposition thicknesses of 1KÅ, 2KÅ, and 4KÅ, combined with a standard timed TEOS etch on the LRC4526 XL platform.

3.5 Thin PECVD Oxide

Following spacer formation, the top oxide of the ONO gate dielectric stack will have been completely removed because of the nature of the etch process. The top oxide

must be reformed due to ITO's tendency to reduce in the presence of nitrogen and its poor adhesion to silicon nitride. In order to avoid subjecting the ITO to an extended high-temperature oxidation in a hydrogen-containing environment, deposition of the top oxide is undertaken by PECVD of a thin TEOS layer. Electrical integrity of the gate stack must be supported primarily by the bottom thermal oxide layer and the silicon nitride layer (which also serves as a diffusion barrier), with the top oxide serving primarily as an adhesion layer for the ITO.

Thin oxide development was undertaken in a 150 mm Applied Materials P-5000 TEOS PECVD platform. Designed mainly for thicker passivation films, the deposition rate had to be slowed considerably in order to allow reasonable process control of a film with a target thickness of approximately 100 Å. To accomplish this, TEOS gas flow was diluted considerably in oxygen, allowing oxides in the thickness range of 50—200 Å with reasonable uniformity to be obtained. From this general process window, a factorial experiment was designed around the three main factors of oxygen flow, TEOS flow, and deposition time, detailed in Appendix B: Thin TEOS Film Designed Experiment. Depositions were run on blanket-deposited wafers containing a thermal oxide and LPCVD nitride film, mirroring the standard process flow. Measurements were made on a KLA-Tencor UV1280SE using appropriate ellipsometric models, and nine measurement sites per wafer. Success was determined by obtaining spectroscopic ellipsometry readings after "reoxidation" that were comparable to readings from the ONO stack prior to processing.

3.6 Electrical Testing

Shorts yield and performance was tested using an automated test system which forced a current of 10 μA through the first-level and second-level bond pads while measuring the resulting potential difference. First-level and second-level electrode to substrate resistance was measured in a similar manner, forcing a current through one of the bond pad connections to each of the electrode phases and out the substrate contact, again measuring the resulting potential difference.

Chapter 4 reviews and discusses the results of these studies and the overall process integration to fabricate an all-ITO CCD.

Chapter 4

Results and Discussion

4.1 ITO Deposition

Following blanket deposition of ITO on wafers with alignment marks, SEM inspection of various defects was performed. Each defect of interest was labeled with a letter. Defect A, roughly 4 μm in diameter, had an appearance similar to that of a dielectric flake, as though from the chamber walls or the target, as shown in Figure 8. FIB images demonstrate that the particle was sitting on top of the ITO film, indicating that it fell on the wafer at the very end, or following completion, of the deposition process. This would indicate flaking from the chamber walls or the target.

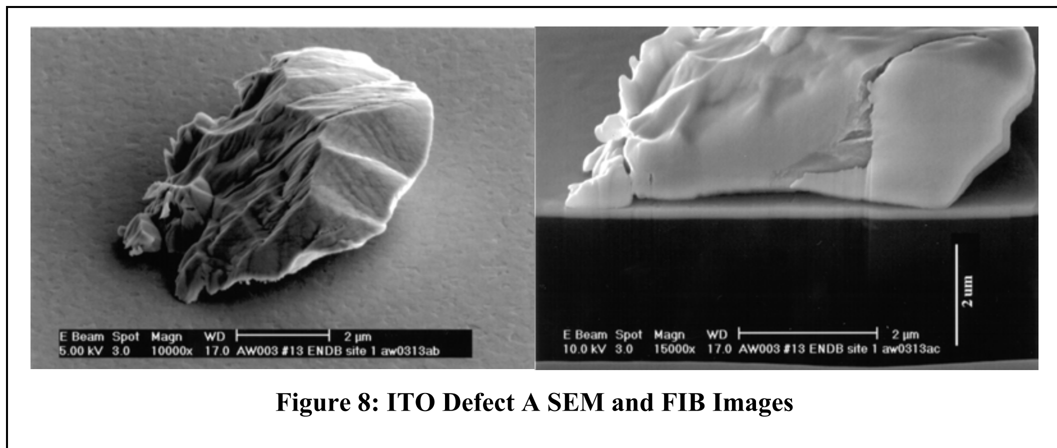

Figure 8: ITO Defect A SEM and FIB Images

EDS analysis of the particle showed a composition of mostly indium/tin and oxygen. Analysis of the film showed indium/tin and oxygen as well, combined with a significant silicon peak, much stronger than that of the particle, which was expected

given the thickness of the sample and the interaction volume of the electron beam. A comparison spectra from the particle and the substrate is shown in Figure 9. Note that indium and tin are virtually indistinguishable at these resolutions.

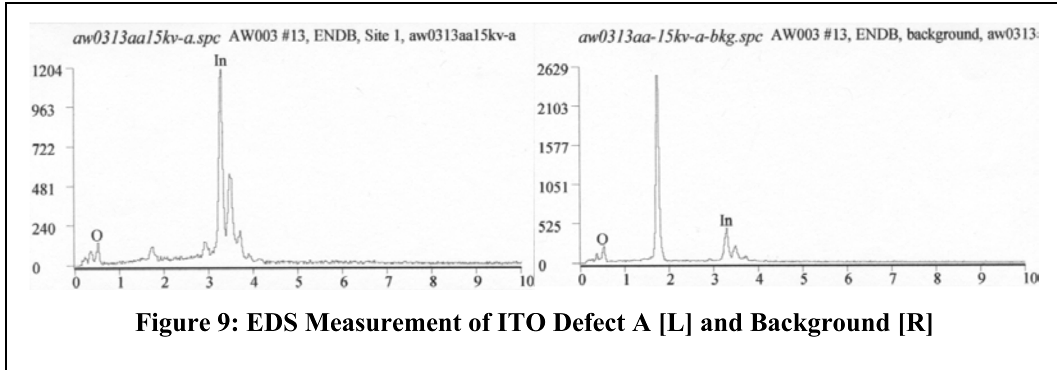

Figure 9: EDS Measurement of ITO Defect A [L] and Background [R]

Defect B exhibited similar characteristics, largely indicative of a flake from the chamber walls or target falling on the sample. A close examination of the SEM and FIB images revealed a slight grain structure, with grains appearing to be 100–400 nm in size, as observed in Figure 10. This is consistent with previous ITO grain structure studies [47]. The lighter rectangular area on the left-hand side of the FIB image was a result of slight sample charging from a higher resolution image created prior to obtaining the FIB image. EDS analysis for this defect was almost identical to that made for Defect A, as expected if the two particles were caused by the same mechanism.

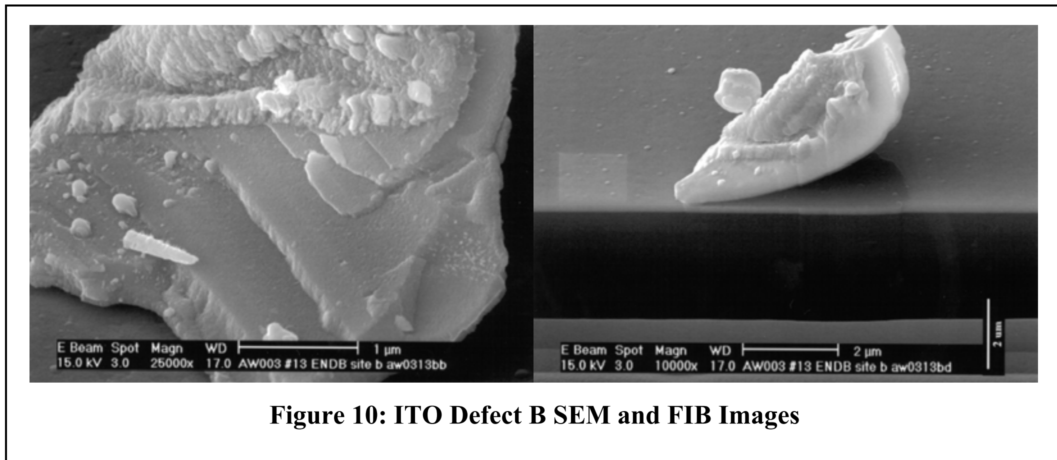

Figure 10: ITO Defect B SEM and FIB Images

Inspection of the PVD chamber while defect performance was poor led to two major observations. First, the edge of the ITO target was discolored and built up with what appeared to be a powdery residue. This build-up of what may have been an insulating film could lead to arcing and particle formation. Second, the target was covered with tiny black nodules in random patterns, slightly raised from the target. These "black nodules" are typically characterized as sub-oxide regions characteristic of ITO sputtering, which could cause arcing which results in increased particle levels. Given that most of the particles appear to be due to flaking mechanisms, particle reduction efforts focused on improving film adhesion to the chamber sidewalls while reducing arcing.

Both of the proposed defect mechanisms (arcing from both black nodules and target insulator build-up, as well as chamber flaking) were addressed. Arcing, believed caused by standard target poisoning as a result of oxidation forming a dielectric coating, was addressed by two means. First, conditioning processes were devised to return the target to a pristine condition during maintenance events. Second, the frequency of the RPG power supply opposite-phase pulses was increased, increasing the preferential re-sputtering of any insulating material building up on the target before it could collect enough charge to cause micro-arcing in the chamber. Chamber flaking was improved by revising target condition procedures and refining chamber cleaning procedures. The combination of the improved cleaning and conditioning processes, along with the increased RPG frequency, resulted in a drastic reduction in defects in as-sputtered ITO

films. Figure 11 shows the relative improvement in particle defect densities that resulted from this work.

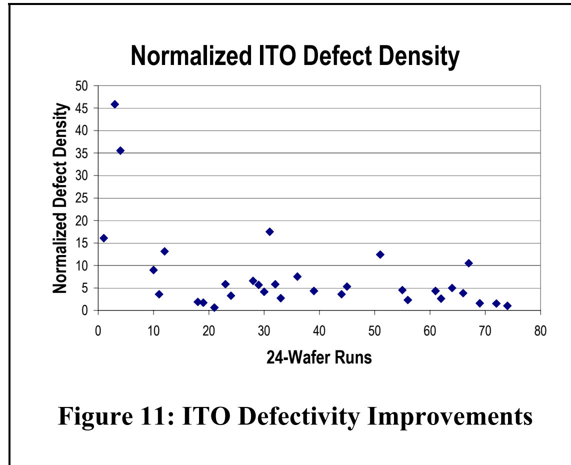

Figure 11: ITO Defectivity Improvements

4.2 Hard Mask Etch

First-pass wafers using the proposed baseline process exhibited adequate etch characteristics with TEOS sidewall angles ≥87°. Pre- and post-etch vertical SEM micrographs (VSEMs) are shown in Figure 12 and Figure 13. Resist appears mostly undamaged, sidewalls are near vertical, and ITO damage appears negligible, indicating original etch conditions were adequate for the required task.

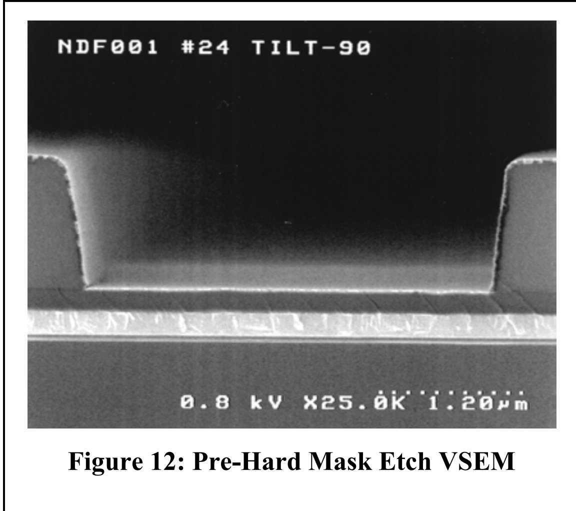

Figure 12: Pre-Hard Mask Etch VSEM

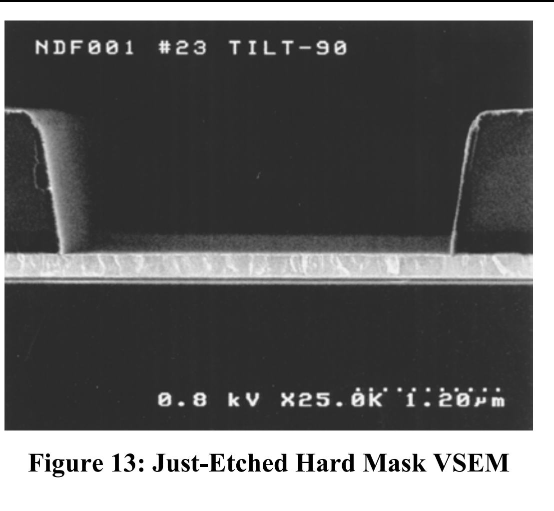

Figure 13: Just-Etched Hard Mask VSEM

4.3 First-level ITO Etch

In the initial first-level ITO etch, the hard-mask etch was followed by a brief plasma de-scum to remove any residual polymer deposits over the exposed ITO, prior to ITO etch, leaving a mask of photoresist and TEOS oxide. However, this process resulted in significant edge roughness, as depicted in Figure 14 and Figure 15.

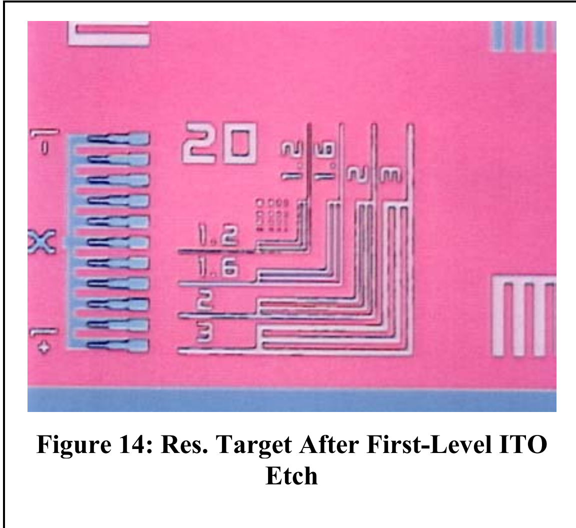

Figure 14: Res. Target After First-Level ITO Etch

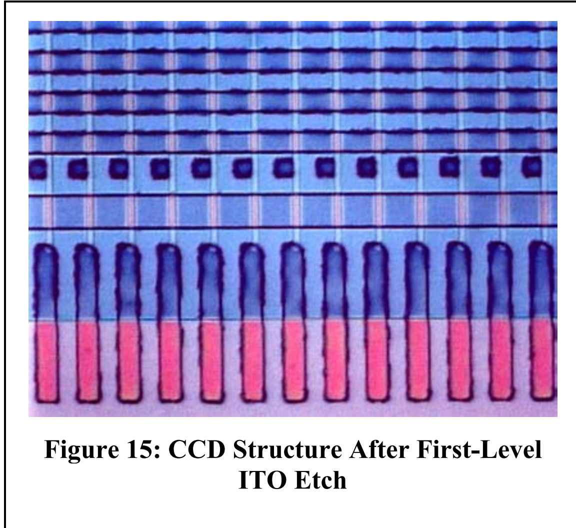

Figure 15: CCD Structure After First-Level ITO Etch

In order to better understand whether this roughness, nicknamed the “mouse-bite” phenomenon, was an artifact of photoresist reticulation or had transferred into the first-level ITO pattern, SEM images shown in Figure 16 and Figure 17 were obtained.

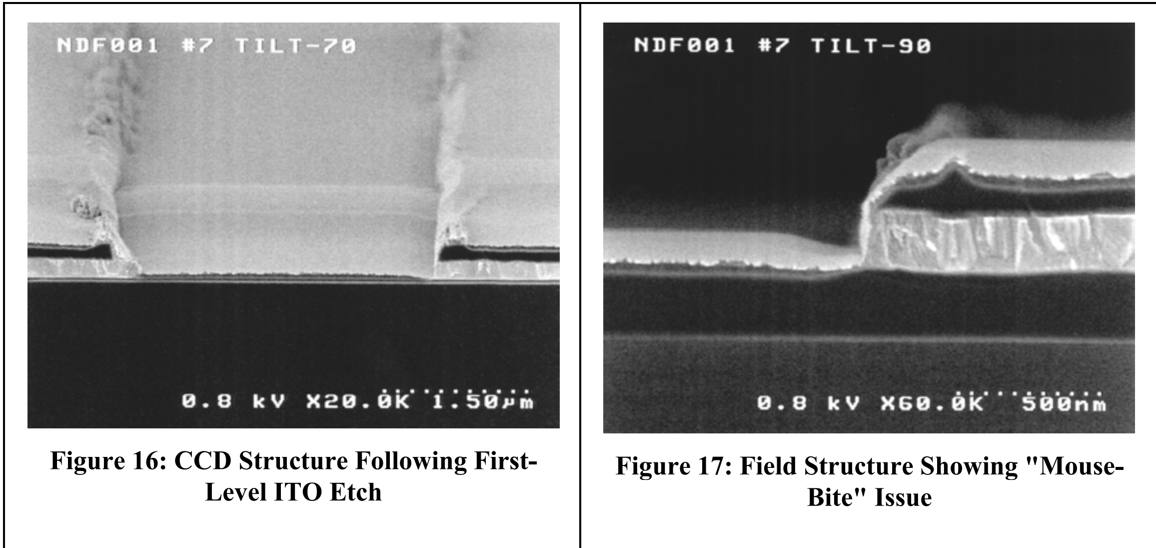

Figure 16: CCD Structure Following First-Level ITO Etch

Figure 17: Field Structure Showing "Mouse-Bite" Issue

Clearly, the resist is degrading along the sidewalls and either pulling back or falling into the previously defined edges of the etch regions, resulting in inconsistent sidewall etch profiles. In order to clean up the first-level ITO edge definition, the hard-mask etch was supplemented with a comprehensive resist ash and strip sequence (which included buffered oxide etchant) prior to the ITO etch, utilizing the TEOS film as a hard mask without any photoresist. The ITO etch endpoint algorithm was modified due to the different in-chamber chemistry, providing much improved results,as depicted in Figure 18 and Figure 19. The risk in this revised process was a possible reduction in the thickness of the TEOS insulating layer over the first-level electrode, leading to possible first to second-level electrode shorts, if the edges of the first-level electrode are left exposed following the spacer etch.

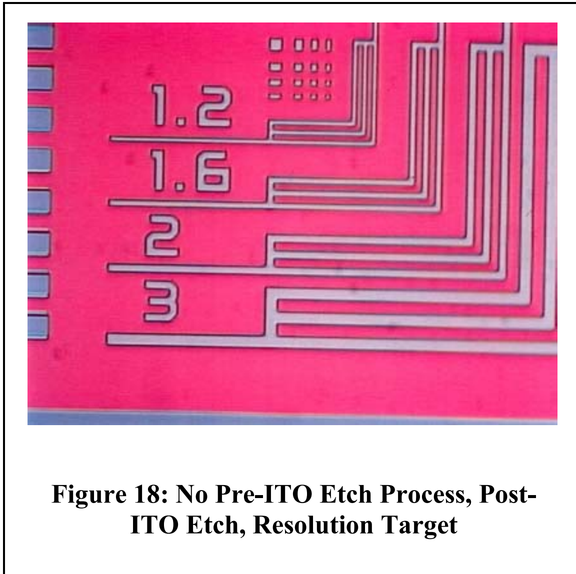

Figure 18: No Pre-ITO Etch Process, Post-ITO Etch, Resolution Target

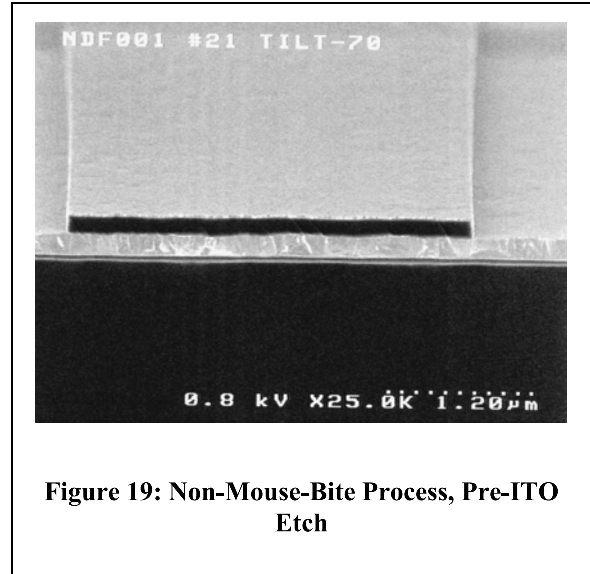

Figure 19: Non-Mouse-Bite Process, Pre-ITO Etch

4.4 Spacer Etch

Using a fixed-etch time for spacer formation proved inadequate, as a few seconds over or under etching left either too thin or thick a gate dielectric, as shown in Figure 20. This variability in dielectric thickness under the second-level electrode could lead to loss of control of potential well depths in the barrier regions, resulting in inefficient charge transfer during operation of the device.

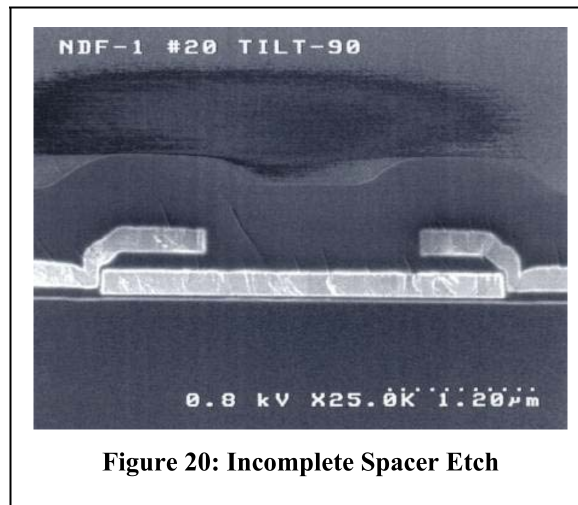

Figure 20: Incomplete Spacer Etch

Further etch development was undertaken in order to obtain improved oxide-to-nitride etch selectivity while finding an etch that would be compatible with automated endpoint detection schemes. Using a starting point of a previously developed oxide-contact etch designed to stop on a nitride film for back-end processing [48], as shown in Table 2, the new spacer etch process resulted in an etch selectivity of 5:1 TEOS oxide to nitride and a TEOS etch rate of approximately 2750 Å/min.

Parameter	**Original Contact Etch**	**Revised Spacer Etch**
Pressure	20 mTorr	26 mTorr
CHF3 Flow	0 sccm	0 sccm
C4F8 Flow	8 sccm	8 sccm
O2 Flow	7 sccm	7 sccm
Ar Flow	120 sccm	120 sccm
RF Upper Electrode	1000 W	500 W
RF Bias Electrode	1000 W	500 W
Gap Height	1.45 cm	1.45 cm
Backside Helium Pressure	15 Torr	15 Torr
Upper Electrode Temp	30°C	40°C
Lower Electrode Temp	20°C	10°C

Table 2: Comparison of Contact and Revised Spacer Etch Parameters

Etch selectivity was obtained by processing at such a low fluorine-to-carbon ratio that the plasma process hovers at the boundary between etching and polymer formation [49], depicted in Figure 21. The high bias applied to the lower RIE chamber electrode slightly sputters the thin film. While sputtering the SiO_2 layer, oxygen is released into the ambient, scavenging-free carbon and increased the overall fluorine-to-carbon ratio [50], pushing the etch past polymerization and into the etch regime. Once the etch reaches the nitride, however, the only oxygen liberated during the etch is from the continued etching of the sidewall spacer, reducing the overall oxygen level in the chamber and lowering the fluorine-to-carbon ratio. This pushes the plasma process back

into the region of protective polymer formation, slowing the etch rate of the silicon nitride [51].

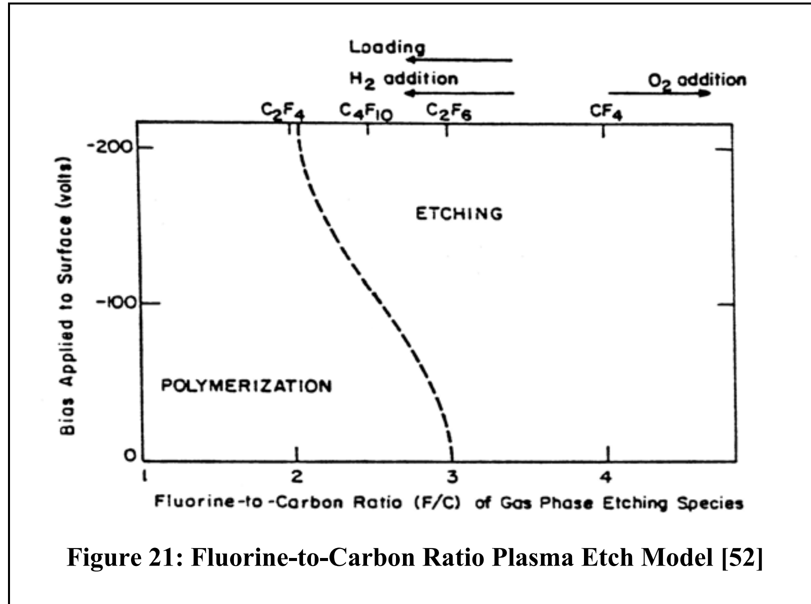

Figure 21: Fluorine-to-Carbon Ratio Plasma Etch Model [52]

The reduction of oxygen in the chamber as the nitride is uncovered slows the formation of CO, resulting in a decreased intensity of CO plasma emission lines at 486.5 and 519.8 nm. This decrease in signal intensity can be used in an automated endpoint detection system. An algorithm was developed in which the intensity of the CO line at 519.8 nm was sampled while the RF was applied to the RIE chamber. Following a 5 second delay time for plasma ignition and 5 seconds for intensity normalization, endpoint is achieved when a line intensity of <95% of the normalized line intensity is observed. Following endpoint detection, etching continues for 15% of the main etch endpoint time to account for non-uniformities in processing. A sample endpoint chart from a device wafer is shown in Figure 22.

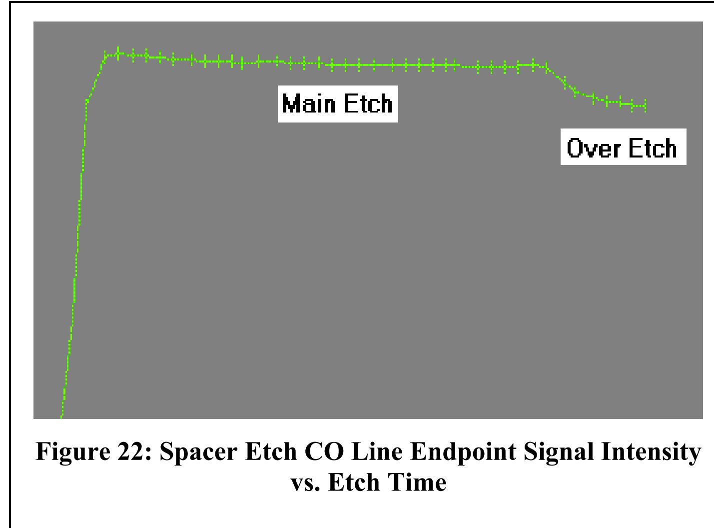

Figure 22: Spacer Etch CO Line Endpoint Signal Intensity vs. Etch Time

Further optimization of this process was not practical due to the nature of the etch itself. Since the etch operates in a regime right at the etch/polymerization boundary, designed experiments around these process conditions are likely to push the process fully into the polymerization regime. This would result in excessive polymer build up inside the chamber, leading to clogging of gas inlet ports and high defectivity, resulting in excessive equipment downtime.

4.5 Thin PECVD Oxide

Using the designed experiment framework detailed in Appendix B: Thin TEOS Film Designed Experiment, R^2 values of greater than 99% for the mean film thickness and greater than 44% for the film thickness standard deviation were obtained. This led to a choice of optimum operating conditions at a deposition time of 7.5s, a TEOS flow of 75 sccms, and an oxygen flow of 700 sccms, resulting in a film with a target thickness at deposition of 100 Å and a film thickness non-uniformity of less than 5% standard

deviation across the wafer. Wafer-to-wafer repeatability was adequate as measured by repetitions of the centerpoint.

4.6 Generation 1 Integration

The first module in the process flow, named the ND-WFR.A1 module, has the sole purpose of pulling the appropriate wafers, starting them on their way in the fabrication facility, and scribing them with appropriate run and wafer numbers.

Once the wafers are started in the fab, they immediately enter the active/ONO module, designed to begin the formation of the ONO gate dielectric stack while simultaneously forming the active and field isolation regions. Wafers are first run through a clean to remove any residual contamination and particles from the scribe area prior to entering an oxidation furnace for growth of a dry thermal oxide, forming the bottom layer of the ONO stack. Actual oxidation thickness and uniformity was measured on the KLA-Tencor UV1280 system.

Following oxidation, wafers undergo an LPCVD silicon nitride deposition, with deposition thickness and particles added measured on a monitor wafer that travels with the run through this step. The run enters the microlithography area for lithographic patterning of the active area using standard photoresist coat, expose, and develop steps. Wafers are inspected visually for proper patterning prior to release from lithography.

The active pattern is transferred from the photoresist into the silicon nitride using a fluorocarbon-based plasma etch. Photoresist and polymer from the plasma etch are removed in a plasma ashing step (combustion of organics in an oxygen plasma) prior to a wet clean to remove any remaining particles or residue. Immediately following the clean, the wafers undergo a field oxidation in a pyrogenic steam environment, forming the thick

field oxide region in areas where nitride was removed, as shown in Figure 23. Simultaneously, a thin film of oxide over the remaining nitride is grown, serving as the top oxide layer of the ONO gate dielectric stack for the first-level electrodes.

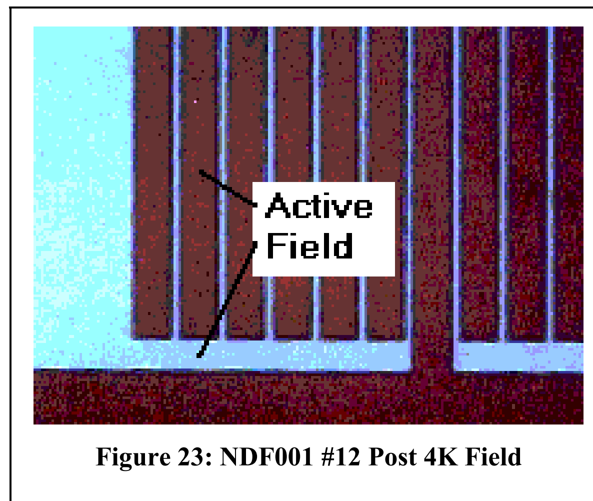

Figure 23: NDF001 #12 Post 4K Field

Next, the wafers enter the ITO module in which the first-level ITO electrodes are formed. The module launches with physical vapor deposition of the ITO electrode, followed by PECVD deposition of a 2000 Å TEOS oxide, which will serve to insulate the top surface of the electrode from the second-level electrode later in the process. Wafers re-enter lithography to create the first-level electrode pattern, as shown in Figure 24. This pattern is transferred into the TEOS oxide by means of a dry etch.

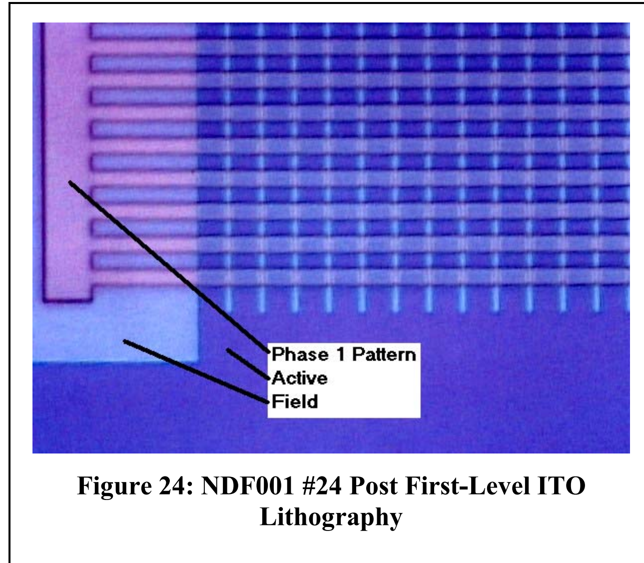

Figure 24: NDF001 #24 Post First-Level ITO Lithography

Wafers are run through a plasma photoresist strip and a series of chemical cleans and plasma "de-scum" processes to remove any organic residues on horizontal ITO services that would serve as unwanted "micro-masks" prior to etching of the ITO. The ITO was etched in a standard parallel-plate, plasma-etch chamber and polymeric residues were removed in a subsequent ash/clean cycle. Post-etch device layout is shown in Figure 25.

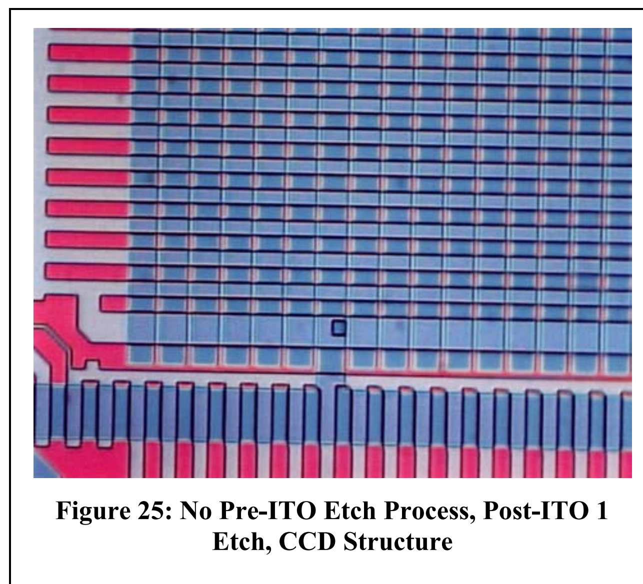

Figure 25: No Pre-ITO Etch Process, Post-ITO 1 Etch, CCD Structure

Following creation of the first-level electrode pattern, the wafers enter the spacer module in which a TEOS layer is conformally deposited by PECVD across the entire wafer, and an anisotropic plasma etch is used to create an insulating sidewall spacer along the edges of the Phase 1 pattern, stopping on the nitride layer of the ONO stack. Following completion of the spacer etch, SEM micrographs indicated the upper corner regions of the first-level ITO electrode were left exposed. This will form shorts following deposition of the second-level ITO electrode, as shown in Figure 26.

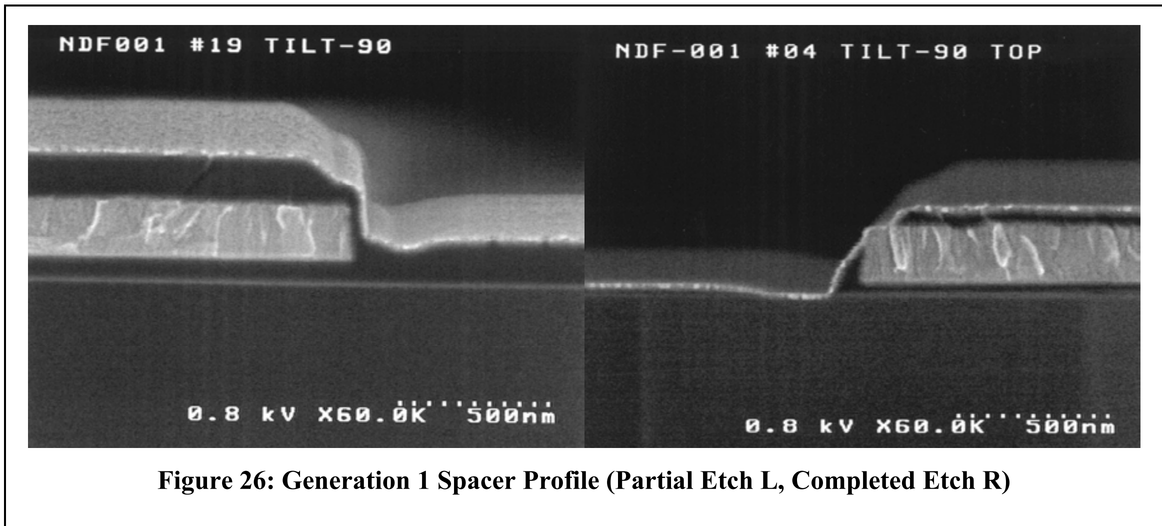

Figure 26: Generation 1 Spacer Profile (Partial Etch L, Completed Etch R)

The uninsulated corners were believed to result from depositing the spacer TEOS layer with too thin an oxide layer over the ITO electrode. This top insulating TEOS layer was originally deposited immediately following deposition of the first electrode. Remediation of the mouse-bite effect, which required an added clean sequence including HF, rendered the thickness of this top oxide layer significantly less than originally anticipated. It was believed that increasing the thickness of this top oxide at the deposition stage from 2000Å to 4000Å would provide a sufficient process window to avoid such issues in the Generation 2 process flow.

Despite the advance knowledge that the first-generation process flow would yield a tremendous number of shorts, the run was continued in order to set up the remaining processes and verify test conditions.

Finishing the spacer module, the top oxide of the ONO stack was re-deposited, this time using a thin TEOS oxide process to insulate the ITO layer from the underlying nitride. Following thin TEOS deposition, the run was thermally annealed in order to densify the insulating films prior to deposition of the second-level ITO. Relieving concerns about the stability of ITO in the thermal anneal process, post-anneal optical inspection did not reveal any defect issues, as illustrated in Figure 27.

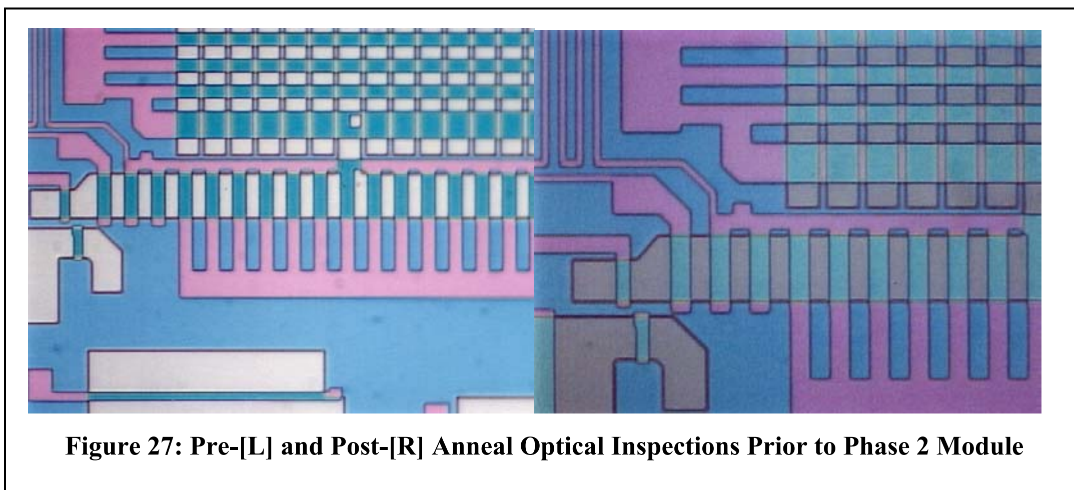

Figure 27: Pre-[L] and Post-[R] Anneal Optical Inspections Prior to Phase 2 Module

Creation of the second-level electrodes was accomplished in a manner similar to that of the first-electrode module. First, ITO is deposited by PVD. Next, instead of entering PECVD for deposition of a TEOS insulating layer, the wafer moves into lithography for patterning of the second-level electrodes. Following lithographic patterning, the ITO is plasma etched as before, followed by resist and polymer removal in standard ash and clean processes. A finished device is shown in Figure 28. As predicted earlier, shorts were observed between the first and second-level electrodes at the upper

corners of the first-level ITO because of insufficient oxide thickness above the first-level electrode.

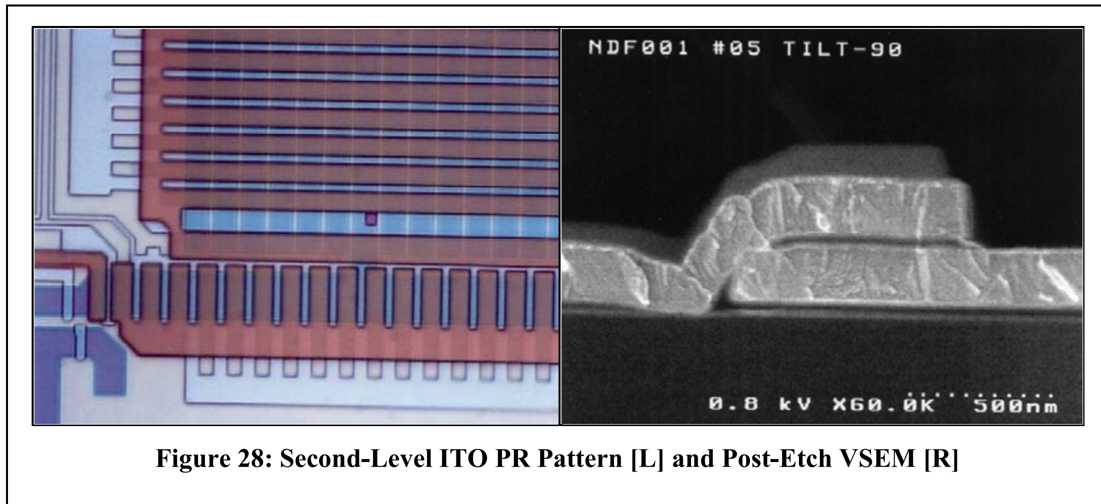

Figure 28: Second-Level ITO PR Pattern [L] and Post-Etch VSEM [R]

Wafers entered the contact module, which began with a planarizing PECVD deposition and etchback process, which leaves a thick TEOS oxide over the entire wafer. The TEOS film is densified in a thermal anneal, prior to contact lithography in which openings are defined to both the first and second-level electrodes. Following lithography, contact openings are transferred from the photoresist through the TEOS oxide layer by means of a standard fluorocarbon RIE step. Figure 29 shows a cross-section of a via.

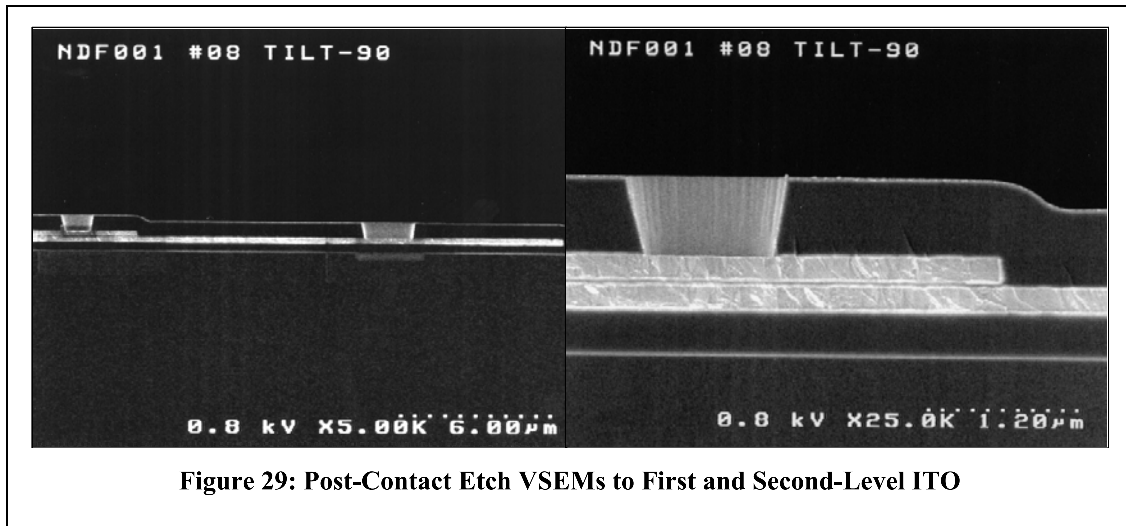

Figure 29: Post-Contact Etch VSEMs to First and Second-Level ITO

Photoresist was ashed prior to a resist clean, completing the contact module. The process ends with the metal module in which the final metallization is deposited and lithographically patterned. The metal lithographic pattern is transferred into the metal by means of a chlorine-based magnetically enhanced RIE process (MERIE). Following metal etch, the photoresist is ashed, wafers are cleaned, and the wafers exit the fab for testing. A metallized CCD is shown in Figure 30.

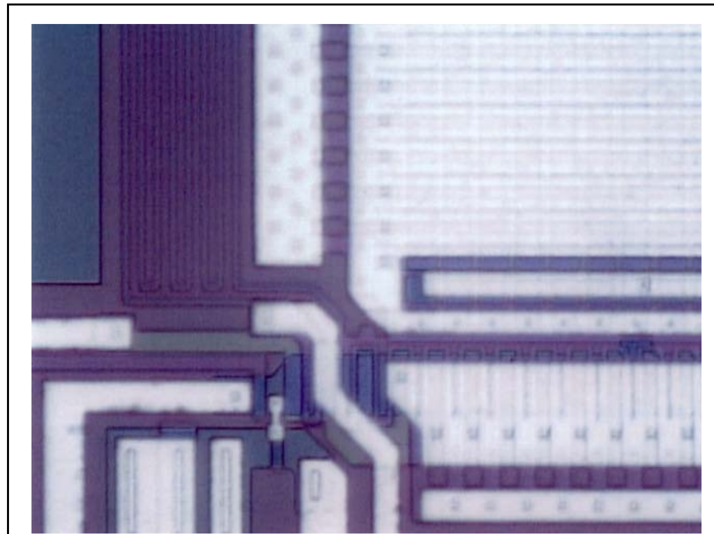

Figure 30: Patterned Metallization Prior to Device Testing

Electrical testing of completed wafers indicated that shorting was widespread, as expected, based on cross-sectional results depicted previously in Figure 28R. As seen in Figure 31, several wafers indicate some isolation between levels, however, predominantly at the high end of spacer deposition, namely 2000 Å. Greater than 90% of the die tested with non-negligible first tio second-level ITO resistance came from one wafer, which received not only a 2000Å spacer deposition, but also experienced pressure control problems during processing at the spacer etch, resulting in significant underetch.

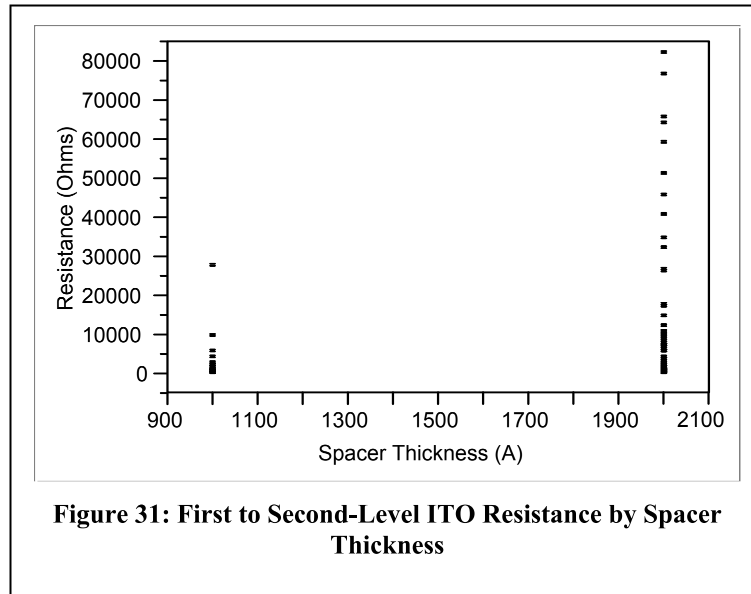

Figure 31: First to Second-Level ITO Resistance by Spacer Thickness

A similar effect was observed with shorting of the second-level electrode to the substrate, measured by forcing a 10 μA current from the substrate connection through the second-level electrode connection. All wafers and die were completely shorted except for the same wafer, further indication of incomplete spacer etch on that single wafer. To conclude, primary failure modes for the initial wafers were twofold. First to second-level electrode shorts were widespread due to insufficient top oxide isolation over the first-level electrode brought about by remediation of the “mouse-bite” effect, as mentioned previously. In addition, a secondary shorting mechanism was observed involving the second-level electrode. Figure 32 shows that a loss of gate dielectric has occurred at the edge of the spacer, allowing the second-level ITO to contact the silicon.

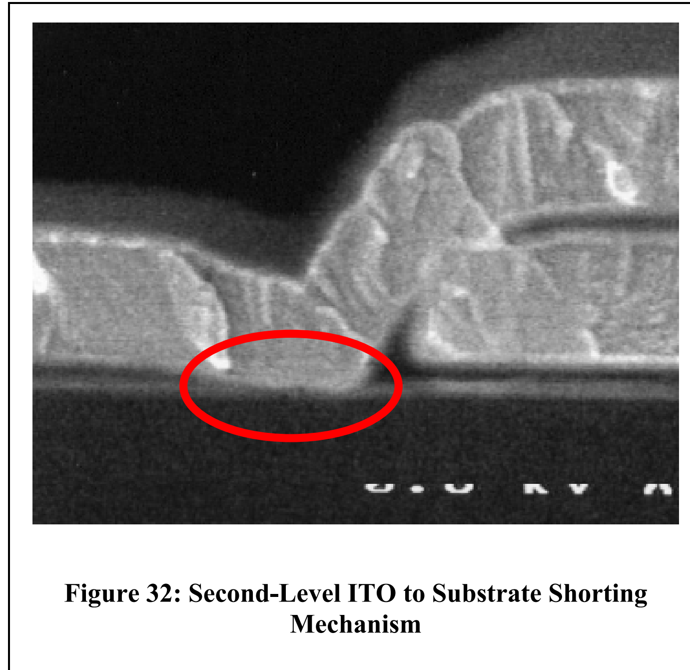

Figure 32: Second-Level ITO to Substrate Shorting Mechanism

4.7 Generation 2 Integration

The second-generation process flow was designed around optimization of the first-level electrode top-oxide and spacer thickness (utilizing the revised spacer etch with automatic endpoint detection) in order to reduce first to second-level ITO shorts. A factorial experimental design was set up with two centerpoints and a single set of replicates to help define the process window for these parameters. Details may be found in Appendix C: Gen 2 Process Experiment and Analysis.

Top TEOS oxide thicknesses were chosen, starting with a 3000Å film as the thinnest top oxide, given that most of the Generation 1 process failed with a 2000Å film. Maximum film thickness was chosen at 5000Å to limit topography of the device. Spacer thicknesses were chosen between 1000Å and 4000Å to provide an adequate process window.

In addition, the second-level electrode to substrate shorting mechanism was also addressed. Reduced gate dielectric thickness in regions directly adjacent to the first-level ITO electrode indicated that micro-loading during the first-level ITO etch reduced the amorphous carbon formation over the gate dielectric, allowing the ITO etch chemistry and ion bombardment to attack the gate dielectric. To reduce this effect, the full ITO etch was split into a two-part etch in which the first part of the etch removes the bulk of the ITO. The etch then switches over to a much-less-aggressive etch regime as the ITO/dielectric interface is approached, leaving the gate dielectric at the edges of the ITO intact.

Testing of second-generation devices was performed using the same test routines as first-generation devices. First to second level ITO shorts exhibited a decidedly bimodal distribution with a large number of runs exhibiting dead shorts (zero resistance) and a second population centered near 15 kΩ, as shown in Figure 33L. Second-level ITO to substrate shorts showed a more normal distribution centered around 200 kΩ, as seen in Figure 33R.

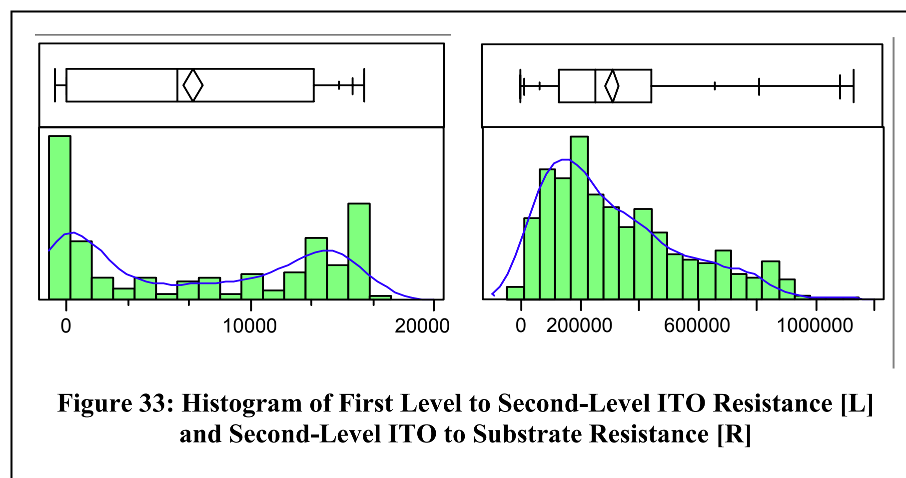

Figure 33: Histogram of First Level to Second-Level ITO Resistance [L] and Second-Level ITO to Substrate Resistance [R]

Closer inspection of the first to second level ITO resistance as a function of the experimental design factors, spacer thickness, and top oxide thickness is displayed graphically in Figure 34. There is a direct correlation between spacer thickness and first to second-level ITO resistance, with thicker spacer oxides resulting in a thicker dielectric between the phases, therefore, a higher resistance. Data indicates that a spacer thickness of 1000Å results in a dead short and is unacceptable. Minimal effect of the top oxide on first to second-level ITO shorting was observed, indicating that the minimum top oxide thickness of 3000 Å is capable of providing sufficient isolation to prevent shorting by the mechanism shown in Figure 28R.

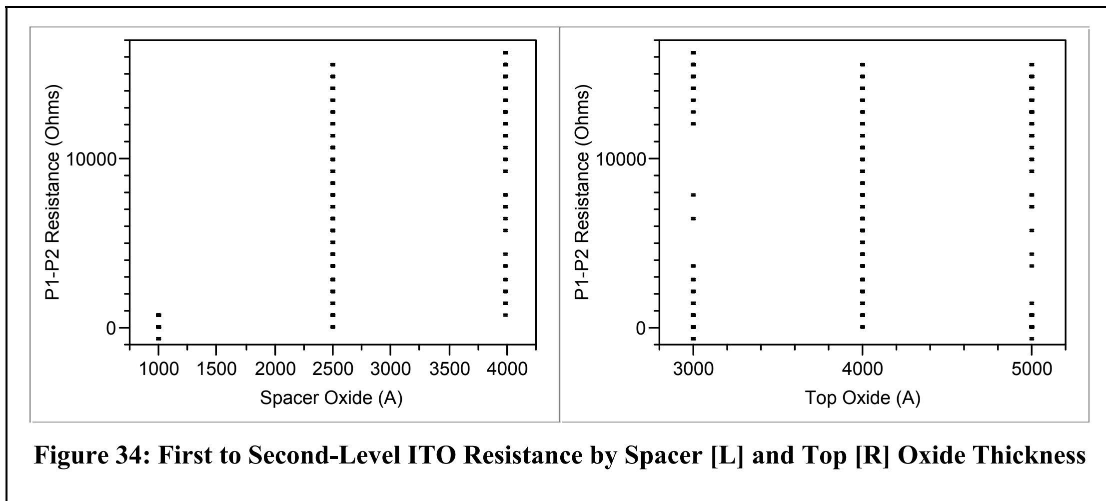

Figure 34: First to Second-Level ITO Resistance by Spacer [L] and Top [R] Oxide Thickness

Parameter estimates indicate that the spacer oxide thickness and top oxide thickness are significant factors in this experiment. This agrees with basic process understanding that thicker spacer oxide depositions should leave a thicker dielectric layer between the first and second-level electrodes. Top oxide thickness is a known effect on first to second-level ITO resistance as determined from the Generation 1 process flow failure analysis. Effect details indicate that spacer thickness is much more significant than top oxide thickness in determining the resistance between first and second-level

electrodes. Appendix C: Gen 2 Process Experiment and Analysis provides a more detailed analysis of the experimental data.

Examination of second-level ITO to substrate resistance as a function of the experimental parameters, however, revealed that thicker spacer oxides provided improved isolation between the second-level electrodes and the substrate. This is illustrated in Figure 35. This indicates that the shorting mechanism shown in Figure 32 may be partially related to micro-loading during the dielectric spacer etch, and not entirely an artifact of an overly aggressive first-level ITO etch. Further, isolation between second-level ITO and the substrate appears to drop off for increasing top oxide thicknesses. Therefore, there may be a process window between the 2KÅ top oxide thickness of the Generation 1 process and the 5KÅ top oxide thickness of the Generation 2 process in need of further exploration in order to optimize device shorts performance.

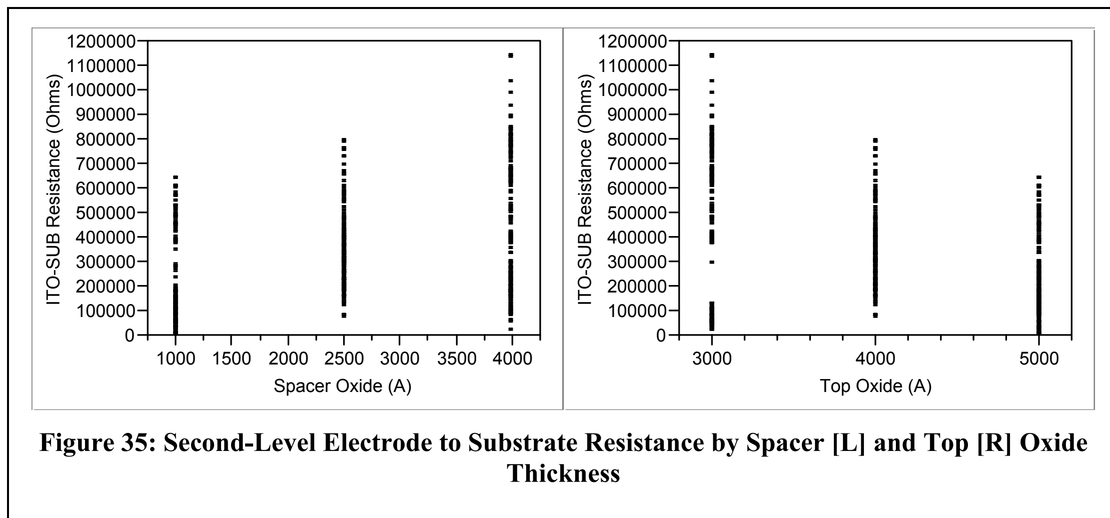

Figure 35: Second-Level Electrode to Substrate Resistance by Spacer [L] and Top [R] Oxide Thickness

Combining both responses, optimized process flow settings for further refinement were generated, with a top oxide thickness of 3KÅ and a spacer thickness of at least 4KÅ. Figure 36 displays the predicted responses for these optimized variables.

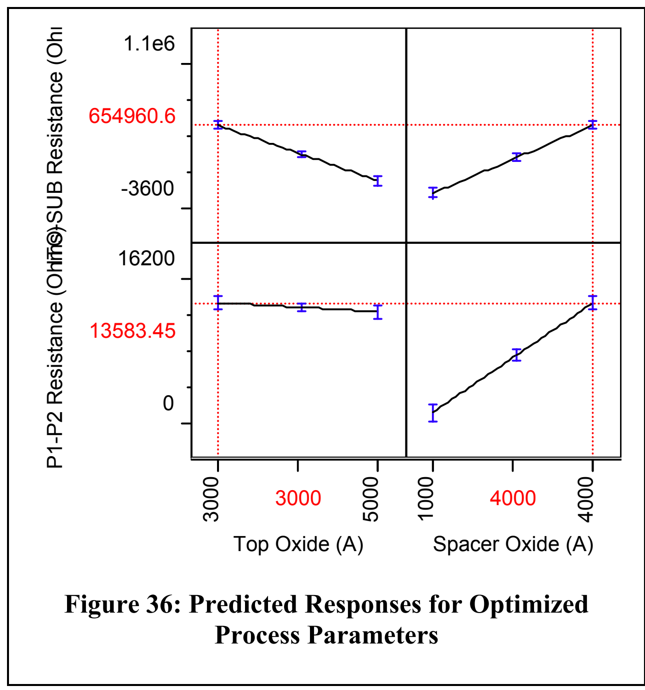

Figure 36: Predicted Responses for Optimized Process Parameters

A cross section of this non-shorted device, shown in Figure 37, exhibits minimal trenching at the edges of the second-level electrodes, coupled with reasonable isolation between the first and second-level electrodes. Experimental analysis and extrapolation indicate that improved isolation (and, therefore, improved shorting performance) should be achievable by increasing the sidewall spacer deposition thickness beyond the 4KÅ limit of this experiment.

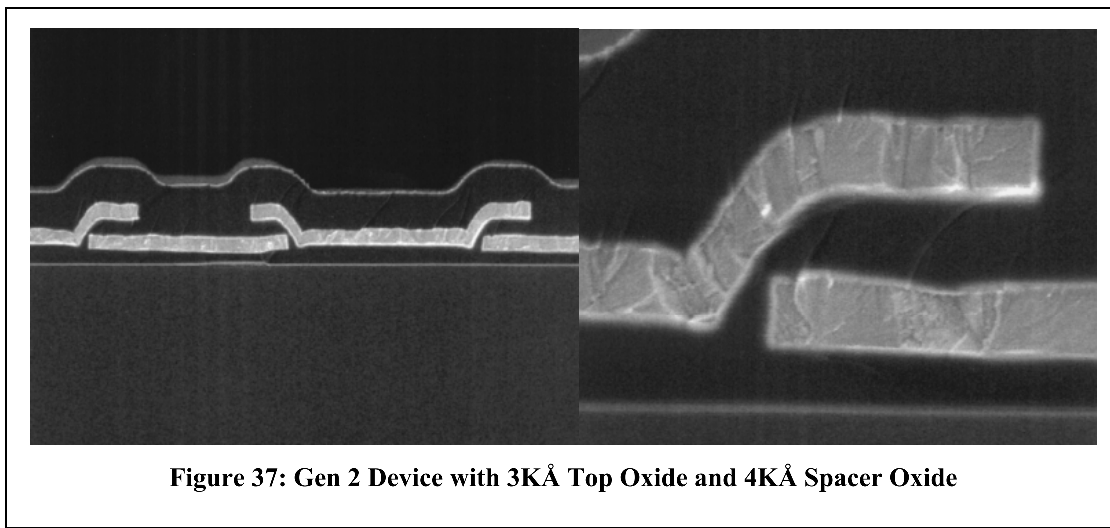

Figure 37: Gen 2 Device with 3KÅ Top Oxide and 4KÅ Spacer Oxide

An increase in the top oxide thickness with the same spacer thickness, from 3KÅ to 5KÅ, results in further erosion of the corners of the hard-mask oxide over the first-level electrode, resulting in a sloped profile for the first-level electrode when combined with the less aggressive and more isotropic first-level ITO etch. This creates a very interesting region where the first and second-level electrodes overlap along a sloped first-level electrode profile. This may present a method of decreasing the inter-electrode spacing while maintaining a reliable dielectric thickness between the electrodes, as shown in Figure 38. The devices of Figure 37 and Figure 38 are very similar to the theoretical device structure demonstrated during SUPREM-IV modeling of the process, the details of which can be found in Appendix A: SUPREM-4 Modeling.

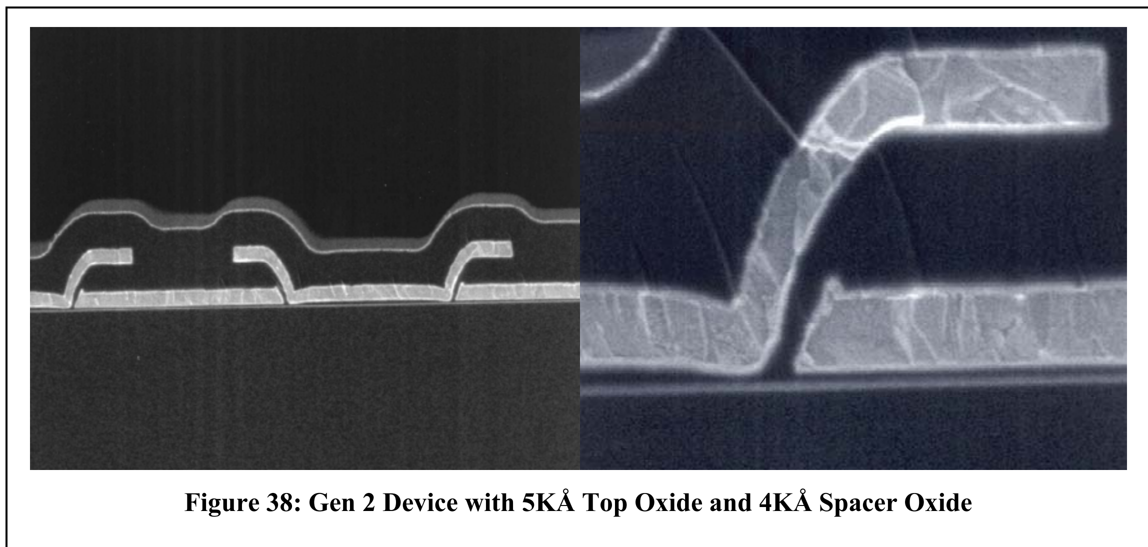

Figure 38: Gen 2 Device with 5KÅ Top Oxide and 4KÅ Spacer Oxide

In an attempt to better understand the second-level ITO to substrate resistance effect and isolate its cause, cross sections were obtained of low-resistance structures, shown in Figure 39. The shorts mechanism appears to produce results very similar to those of the first-generation process flow.

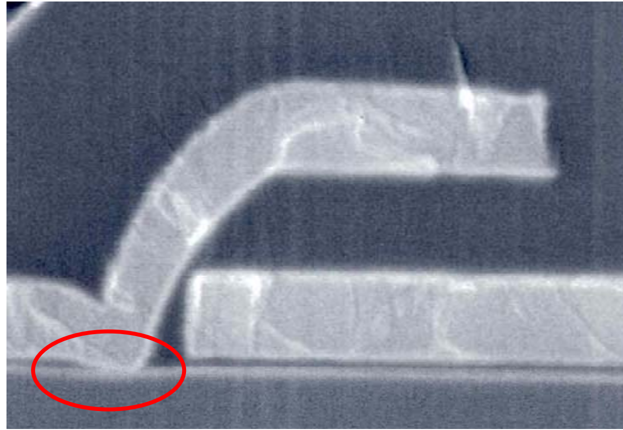

Figure 39: Gen 2 Phase 2 to Substrate Short Mechanism for 2.5K Spacer Process

A subsidiary experiment was performed in which wafers were processed in exactly the same manner with the exception of the first-level ITO over-etch time, which was varied in its duration from the standard (100%) to twice the standard (200%), providing an initial screening for the effect on substrate shorting performance. In general, it was observed that longer over-etch times result in reduced resistance between the second-level electrode and the substrate contact as depicted in Figure 40. This indicated that the ITO over-etch time was a contributing factor to this effect.

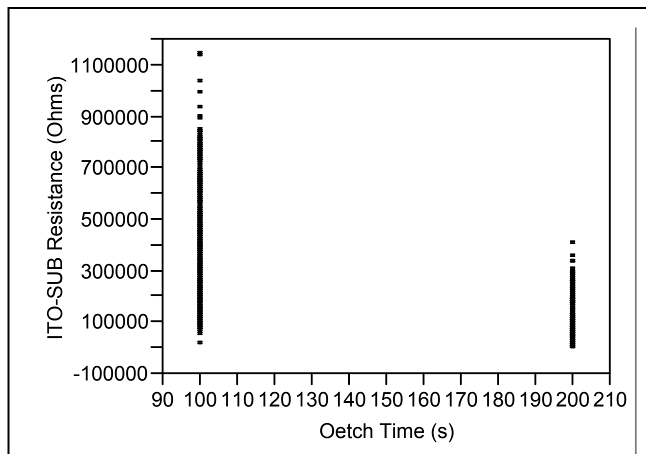

Figure 40: Second Level to Substrate Resistance by First-Level ITO Over-Etch Percentage

The same effect was not observed on devices with thicker spacer oxides, however, indicating that the second-level electrode to substrate shorting mechanism may be a result of both the aggressive first-level ITO electrode etch combined with a micro-loading effect related to the spacer etch. The same region of interest for a device with a 4KÅ spacer thickness is depicted in Figure 41 for comparison purposes. Note that minimal gate dielectric thickness loss is observed for this device. However, like the first-generation process flow, first to second-level ITO shorts can occur as a result of insufficient isolation between the top corner of the first-level electrode and the second-level electrode, as highlighted in Figure 42

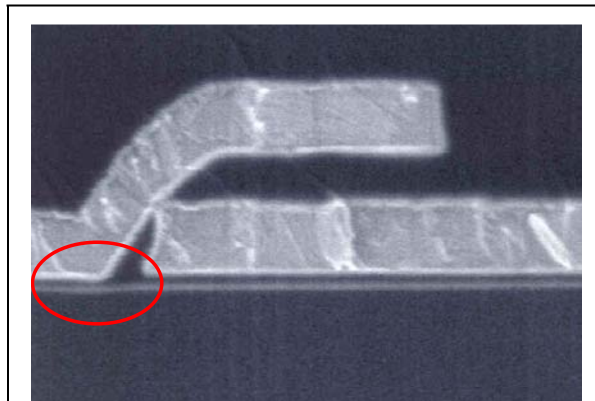

Figure 41: Gen 2 Phase 2 to Substrate Short Region of Interest for 4K Spacer Process

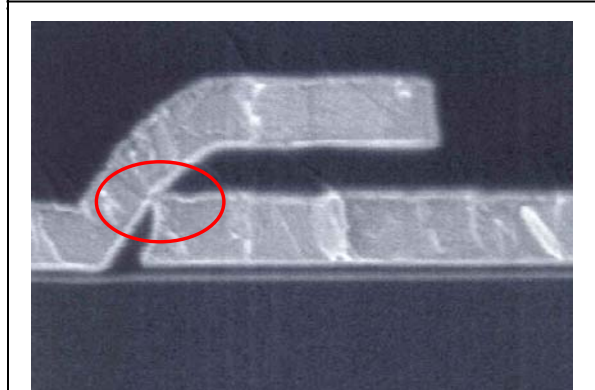

Figure 42: Gen 2 Phase 1 to Phase 2 Shorting Mechanism

Chapter 5

Conclusions and Recommendations

Unit processes were developed for all required non-standard processes associated with this technology, including low-particulate ITO deposition, hard-mask etch, first-level ITO etch, spacer etch, and thin oxide deposition. Each of these unit processes was developed on standard semiconductor equipment compatible with CMOS production process requirements.

The first-generation devices presented several challenges for successful integration. Initial first-level ITO etch required a clean up of the photoresist prior to etching of the ITO, resulting in an overly thin top oxide over the first-level electrode. A major failure mechanism was identified as a high degree of shorting between the first and second-level electrodes due to this thin top oxide. Secondary failure mechanism was a second-level ITO to substrate short caused by trenching of the gate dielectric.

The second-generation device design included an experiment to screen the effects of the top oxide thickness over the first-level electrode and the spacer deposition thickness with respect to first to second-level ITO shorts. As well, the first-level ITO etch was modified to reduce trenching of the gate dielectric at the edges of the first-level ITO, resulting in a reduction in second-level ITO to substrate shorts. These process modifications resulted in significantly improved overall device performance. The same

failure rate mechanisms were identified, but at significantly reduced levels compared to the first-generation process.

A thick top oxide coupled with the thicker sidewall spacer and a modified first-level electrode etch resulted in a tapered first-level electrode structure. This may prove advantageous in reducing the overall first to second-level electrode spacing while maintaining adequate dielectric integrity between the two electrodes. The positive results exhibited with the second-generation process design indicate that this technology may be suitable for a focused development effort, and should be considered a reasonable path for investigation in the creation of a robust manufacturing process for an all-transparent electrode CCD imager.

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50 “Highly Selective Oxide to Nitride Etch Processes on BPSG/Nitride/Oxide Structures in a MERIE Etcher,” Graf et al., IEEE/SEMI Advanced Semiconductor Manufacturing Conference, 1998, pp. 314–319.

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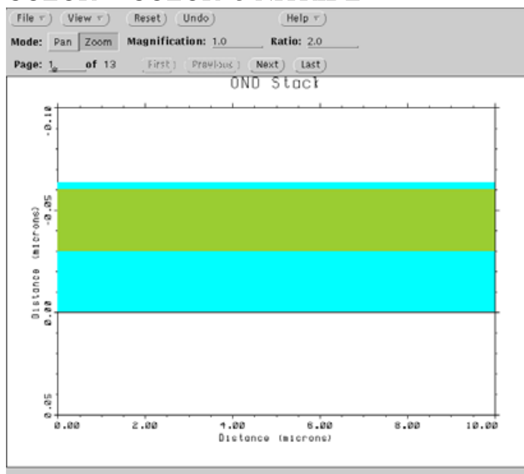
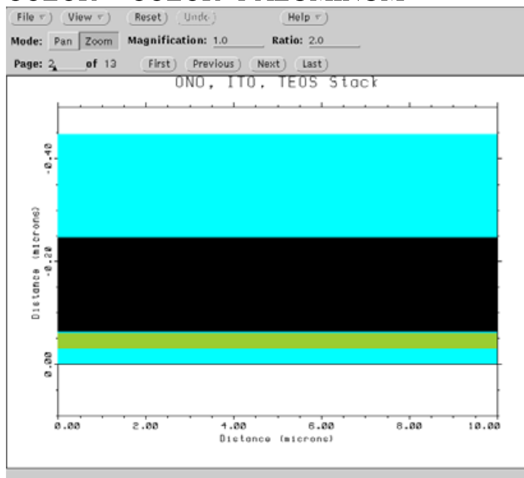
Appendix A: SUPREM-4 Modeling

```
INITIALIZE WIDTH=10 DX=.1 <100> ROT.SUB=0.0 RATIO=1.5 RESISTIV PHOSPHOR=5.5
$  OPTION    DEVICE=PS PLOT.OUT=nozeroox.ps
OPTION    DEVICE=X NORMAL INFORMAT DIAGNOST
$ PSEUDO TWO-PHASE DITO PROCESS Rev 1.0
$
$ Dan Fullerton, 11/27/02
$
$ 115 Full Clean
$
$ 518 Dry Oxidation
DEPOSITION OXIDE SPACES=1 CONCENTR
$
$ 590 LPCVD Nitride
DEPOSITION NITRIDE SPACES=1 CONCENTR
$
$ 533 Ramped Field Ox (grow Top Oxide)
DIFFUSION TEMPERAT=800 T.FINAL=950 TIME=15 INERT
DIFFUSION TEMPERAT=950 T.FINAL=950 TIME=5 DRYO2
DIFFUSION TIME=116.5 TEMPERAT=950 WETO2
DIFFUSION TEMPERAT=950 TIME=5 DRYO2
DIFFUSION TEMPERAT=950 TIME=30 INERT
DIFFUSION TEMPERAT=950 T.FINAL=800 TIME=30 INERT
DEPOSITION OXIDE SPACES=1 CONCENTR
EXTRACT   X=3 OXIDE AREA.EXT PREFIX="Top Oxide Stack After Field  " SUFFIX=um +
 WRITE OUT.FILE=newdog.data
$ END 533 FURNACE RAMPED FIELD OX
$
$ Plot ONO Stack
SELECT    TITLE="ONO Stack"
PLOT.2D   X.MIN=0 X.MAX=10 Y.MIN=-.1 Y.MAX=.05 X.SIZE=0.25 Y.SIZE=0.25 +
 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
COLOR     COLOR=5 OXIDE
COLOR     COLOR=3 NITRIDE
```

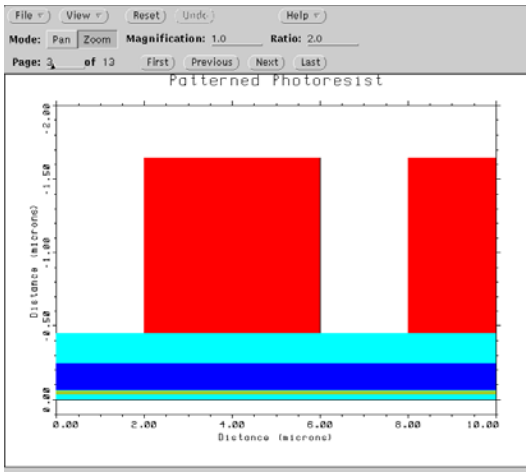



```
$
$ 6530 Deposit ITO
```

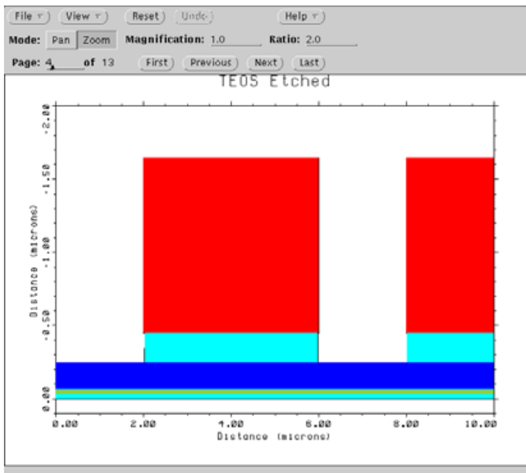
```
$ (Use aluminum for modeling)
DEPOSITION ALUMINUM SPACES=1 CONCENTR
$
$ 938 Deposit TEOS 2K
DEPOSITION OXIDE THICKNES=.2 SPACES=1 CONCENTR
$
$ Plot ONO, ITO, TEOS Stack
SELECT    TITLE="ONO, ITO, TEOS Stack"
PLOT.2D   X.MIN=0 X.MAX=10 Y.MIN=-.5 Y.MAX=.1 X.SIZE=0.25 Y.SIZE=0.25 +
 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
COLOR     COLOR=5 OXIDE
COLOR     COLOR=3 NITRIDE
COLOR     COLOR=1 ALUMINUM
```



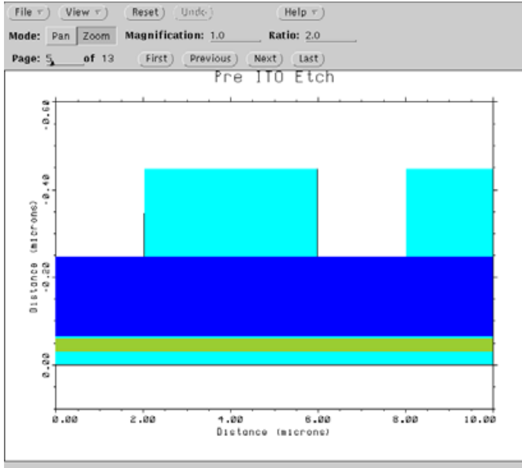

```
$
$ Pattern Photoresist
DEPOSITION PHOTORES POSITIVE THICKNES=1.2 SPACES=1 CONCENTR
ETCH      PHOTORES LEFT P1.X=2 P2.X=2
ETCH      PHOTORES START X=6 Y=-2
ETCH      PHOTORES CONTINUE X=6 Y=0
ETCH      PHOTORES CONTINUE X=8 Y=0
ETCH      PHOTORES DONE X=8 Y=-2
SELECT    TITLE="Patterned Photoresist"
PLOT.2D   X.MIN=0 X.MAX=10 Y.MIN=-2 Y.MAX=.1 X.SIZE=0.25 Y.SIZE=0.25 +
 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
COLOR     COLOR=5 OXIDE
COLOR     COLOR=3 NITRIDE
COLOR     COLOR=4 ALUMINUM
COLOR     COLOR=2 PHOTORES
```



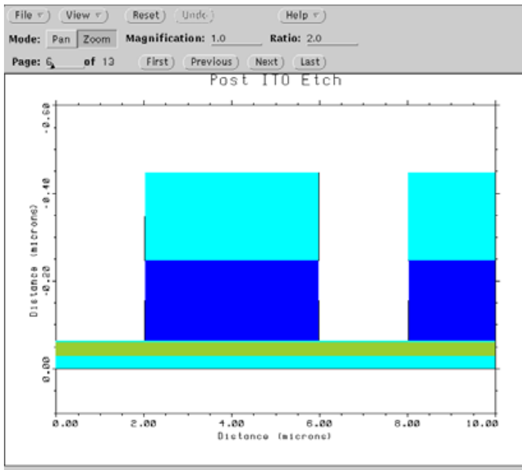

```
$ Etch TEOS, Stop on ITO
ETCH      OXIDE TRAPEZOI ANGLE=87
SELECT    TITLE="TEOS Etched"
PLOT.2D   X.MIN=0 X.MAX=10 Y.MIN=-2 Y.MAX=.1 X.SIZE=0.25 Y.SIZE=0.25 +
 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
COLOR     COLOR=5 OXIDE
COLOR     COLOR=3 NITRIDE
COLOR     COLOR=4 ALUMINUM
COLOR     COLOR=2 PHOTORES
```



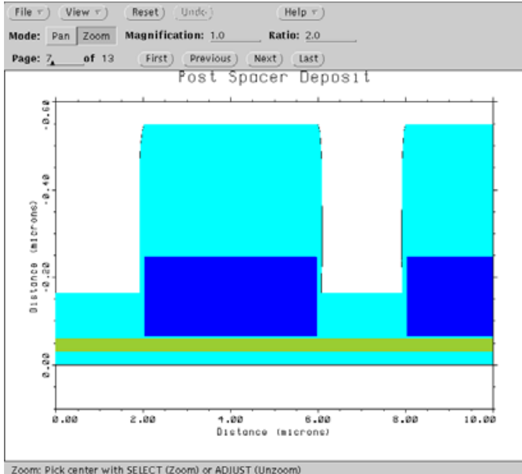

```
$
$ Strip PR
ETCH      PHOTORES ALL
SELECT    TITLE="Pre ITO Etch"
PLOT.2D   X.MIN=0 X.MAX=10 Y.MIN=-.6 Y.MAX=.1 X.SIZE=0.25 Y.SIZE=0.25 +
 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
COLOR     COLOR=5 OXIDE
COLOR     COLOR=3 NITRIDE
COLOR     COLOR=4 ALUMINUM
COLOR     COLOR=2 PHOTORES
```



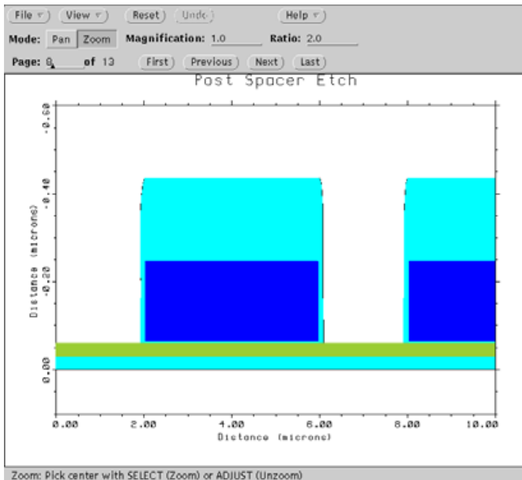

```
$
$ Etch ITO, Stop on Oxide
ETCH      ALUMINUM TRAPEZOI ANGLE=87
SELECT    TITLE="Post ITO Etch"
PLOT.2D   X.MIN=0 X.MAX=10 Y.MIN=-.6 Y.MAX=.1 X.SIZE=0.25 Y.SIZE=0.25 +
 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
COLOR     COLOR=5 OXIDE
COLOR     COLOR=3 NITRIDE
COLOR     COLOR=4 ALUMINUM
COLOR     COLOR=2 PHOTORES
```



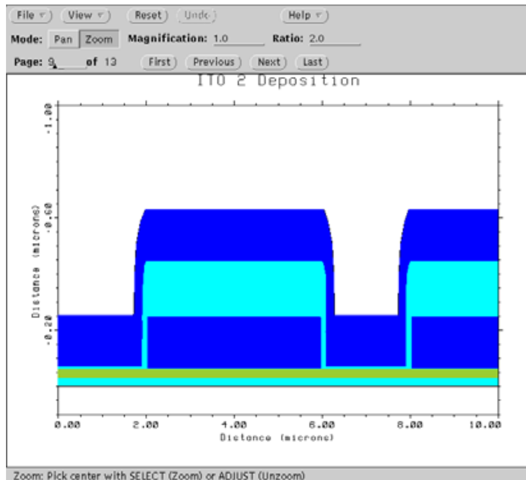

```
$
$ Carbon strip, clean
$
$ Deposit TEOS Sidewall spacer
DEPOSITION OXIDE SPACES=1 CONCENTR
SELECT    TITLE="Post Spacer Deposit"
PLOT.2D   X.MIN=0 X.MAX=10 Y.MIN=-.6 Y.MAX=.1 X.SIZE=0.25 Y.SIZE=0.25 +
 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
COLOR     COLOR=5 OXIDE
COLOR     COLOR=3 NITRIDE
COLOR     COLOR=4 ALUMINUM
COLOR     COLOR=2 PHOTORES
```



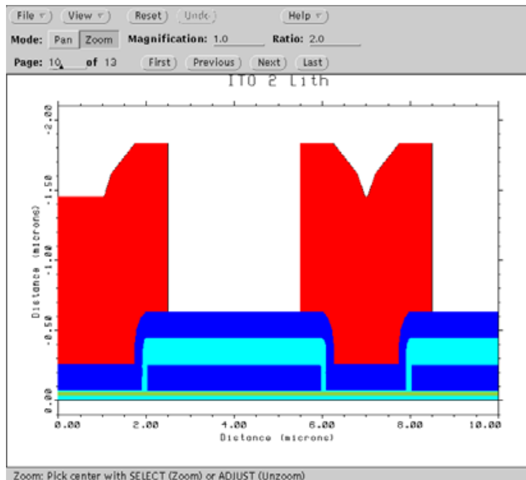

```
$
$ Sidewall Spacer Etch
ETCH      OXIDE TRAPEZOI ANGLE=87
SELECT    TITLE="Post Spacer Etch"
PLOT.2D   X.MIN=0 X.MAX=10 Y.MIN=-.6 Y.MAX=.1 X.SIZE=0.25 Y.SIZE=0.25 +
 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
COLOR     COLOR=5 OXIDE
COLOR     COLOR=3 NITRIDE
COLOR     COLOR=4 ALUMINUM
COLOR     COLOR=2 PHOTORES
```




```
$
$ Clean
IMPLANT   BORON
$ Regrow top oxide?
DEPOSITION OXIDE SPACES=1 CONCENTR
$
DEPOSITION ALUMINUM SPACES=1 CONCENTR
SELECT    TITLE="ITO 2 Deposition"
PLOT.2D   X.MIN=0 X.MAX=10 Y.MIN=-1 Y.MAX=.1 X.SIZE=0.25 Y.SIZE=0.25 +
 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
COLOR     COLOR=5 OXIDE
COLOR     COLOR=3 NITRIDE
COLOR     COLOR=4 ALUMINUM
COLOR     COLOR=2 PHOTORES
```

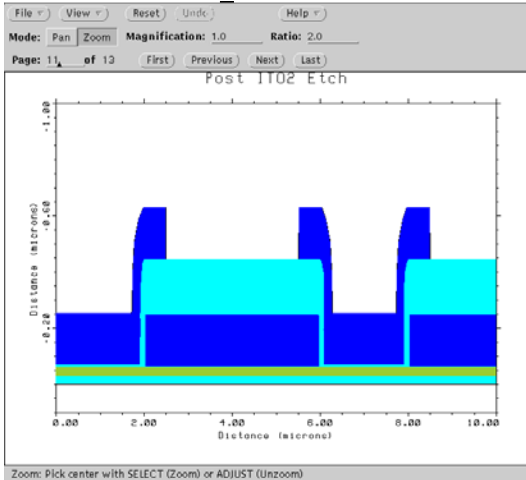



```
$
$ Pattern ITO2
DEPOSITION PHOTORES POSITIVE THICKNES=1.2 SPACES=1 CONCENTR
ETCH     PHOTORES RIGHT P1.X=8.5 P2.X=8.5
ETCH     PHOTORES START X=2.5 Y=-3
ETCH     PHOTORES CONTINUE X=2.5 Y=0
ETCH     PHOTORES CONTINUE X=5.5 Y=0
ETCH     PHOTORES DONE X=5.5 Y=-3
SELECT   TITLE="ITO 2 Lith"
PLOT.2D  X.MIN=0 X.MAX=10 Y.MIN=-2.1 Y.MAX=.1 X.SIZE=0.25 Y.SIZE=0.25 +
 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
COLOR    COLOR=5 OXIDE
COLOR    COLOR=3 NITRIDE
COLOR    COLOR=4 ALUMINUM
COLOR    COLOR=2 PHOTORES
```

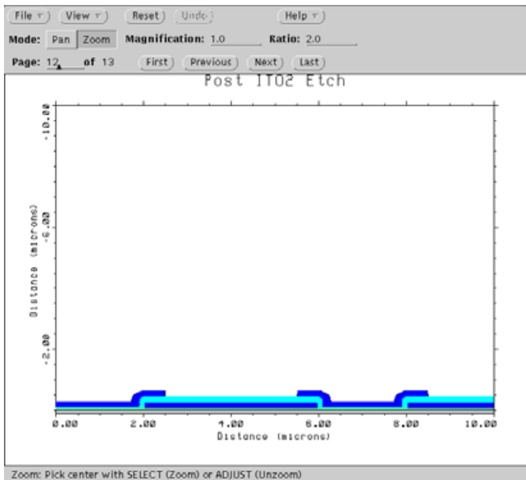



```
$
$ Etch ITO2
ETCH     ALUMINUM TRAPEZOI ANGLE=87
$
$ Strip PR
ETCH     PHOTORES ALL
$
SELECT   TITLE="Post ITO2 Etch"
PLOT.2D  X.MIN=0 X.MAX=10 Y.MIN=-1 Y.MAX=.1 X.SIZE=0.25 Y.SIZE=0.25 +
```

```
 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
COLOR    COLOR=5 OXIDE
COLOR    COLOR=3 NITRIDE
COLOR    COLOR=4 ALUMINUM
COLOR    COLOR=2 PHOTORES
$SOURCE BCONT_CONTROL
```

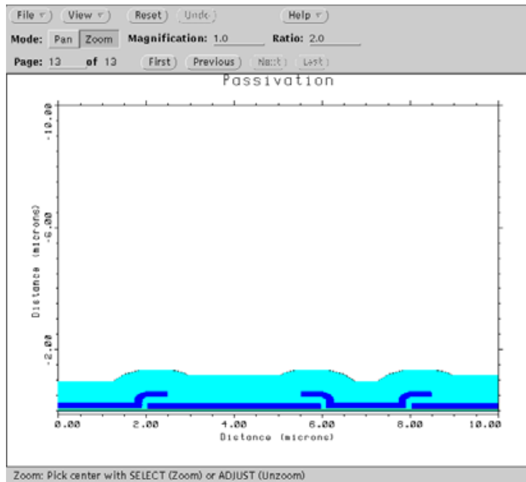



```
$
$ Scale final plot
SELECT    TITLE="Post ITO2 Etch"
PLOT.2D   X.MIN=0 X.MAX=10 Y.MIN=-10 Y.MAX=.1 X.SIZE=0.25 Y.SIZE=0.25 +
 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
COLOR    COLOR=5 OXIDE
COLOR    COLOR=3 NITRIDE
COLOR    COLOR=4 ALUMINUM
COLOR    COLOR=2 PHOTORES
```




```
$
$ Planarize/Encapsulate
DEPOSITION OXIDE SPACES=1 CONCENTR
DEPOSITION PHOTORES POSITIVE THICKNES=1.5 SPACES=1 CONCENTR
SELECT    TITLE="Contact to ITO"
PLOT.2D   X.MIN=0 X.MAX=10 Y.MIN=-10 Y.MAX=.1 X.SIZE=0.25 Y.SIZE=0.25 +
 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
COLOR    COLOR=5 OXIDE
COLOR    COLOR=3 NITRIDE
```

```
COLOR     COLOR=4 ALUMINUM
COLOR     COLOR=2 PHOTORES
```




```
$
$ Contact Etch, stop on ITO
$ ETCH     OXIDE TRAPEZOI THICKNES=1.2 ANGLE=85
$ ETCH     PHOTORES ALL
$ SELECT    TITLE="Contact to ITO"
$ PLOT.2D   X.MIN=0 X.MAX=10 Y.MIN=-10 Y.MAX=.1 X.SIZE=0.25 Y.SIZE=0.25 +
 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
$ COLOR     COLOR=5 OXIDE
$ COLOR     COLOR=3 NITRIDE
$ COLOR     COLOR=4 ALUMINUM
$ COLOR     COLOR=2 PHOTORES
$
$ Deposit TiW, Al
$ DEPOSITION ALUMINUM SPACES=1 CONCENTR
$ SELECT    TITLE="Metal Contacts Patterned"
$ PLOT.2D   X.MIN=0 X.MAX=10 Y.MIN=-10 Y.MAX=.1 X.SIZE=0.25 Y.SIZE=0.25 +
 X.OFFSET=2.0 Y.OFFSET=2.0 T.SIZE=0.4 L.BOUND=1 C.BOUND=1
$ COLOR     COLOR=5 OXIDE
$ COLOR     COLOR=3 NITRIDE
$ COLOR     COLOR=4 ALUMINUM
$ COLOR     COLOR=2 PHOTORES
```

Appendix B: Thin TEOS Film Designed Experiment

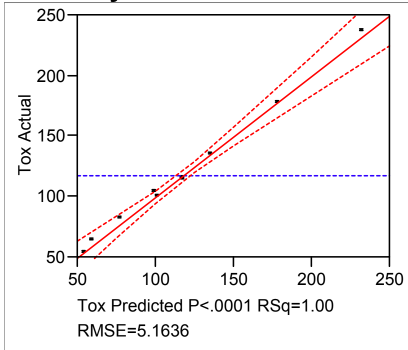
TEOS Thin Film DOE

TEOS Thin Film DOE	
Design	Full Factorial
Model	
Columns (6/0)	
Pattern	
Rows	
All Rows	11
Selected	0
Excluded	0
Hidden	0
Labelled	0

	Pattern	Time	O2	TEOS	Tox	SD Tox
1	---	5	500	50	63.7541	2.9916
2	000	7.5	600	75	114.5168	5.039
3	-+-	5	700	50	52.8146	3.8435
4	000	7.5	600	75	113.6517	4.292
5	--+	5	500	100	133.872	2.2267
6	-++	5	700	100	103.3226	2.9767
7	+--	10	500	50	99.8546	5.5036
8	+++	10	700	100	177.3889	3.1046
9	000	7.5	600	75	113.4997	4.6334
10	++-	10	700	50	81.2326	4.2743
11	+-+	10	500	100	236.9202	4.6235

Table 3: Thin TEOS Deposition Experimental Design

Least-Squares Fit
Response: Mean Top Oxide Thickness
Actual by Predicted Plot



Summary of Fit

RSquare	0.996058
RSquare Adj	**0.990145**
Root Mean Square Error	5.163633
Mean of Response	117.348
Observations (or Sum Wgts)	11

Analysis of Variance

Source	DF	Sum of Squares	Mean Square	F Ratio
Model	6	26949.217	4491.54	168.4551
Error	4	106.652	26.66	Prob > F
C. Total	10	27055.870		<.0001

Lack Of Fit

Source	DF	Sum of Squares	Mean Square	F Ratio
Lack Of Fit	2	106.05043	53.0252	176.1641
Pure Error	2	0.60200	0.3010	Prob > F
Total Error	4	106.65243		0.0056
				Max RSq
				1.0000

Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Intercept	117.34798	1.556894	75.37	<.0001
Time(5,10)	30.204125	1.82562	16.54	<.0001
O2(500,700)	-14.95527	1.82562	-8.19	0.0012
TEOS(50,100)	44.230975	1.82562	24.23	<.0001
Time(5,10)*O2(500,700)	-4.58305	1.82562	-2.51	0.0660
Time(5,10)*TEOS(50,100)	14.0745	1.82562	7.71	0.0015
O2(500,700)*TEOS(50,100)	-7.5649	1.82562	-4.14	0.0143

Effect Tests

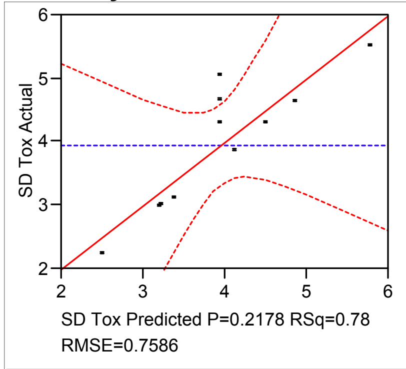
Source	Nparm	DF	Sum of Squares	F Ratio	Prob > F
Time(5,10)	1	1	7298.313	273.7233	<.0001
O2(500,700)	1	1	1789.282	67.1070	0.0012
TEOS(50,100)	1	1	15651.033	586.9921	<.0001
Time(5,10)*O2(500,700)	1	1	168.035	6.3021	0.0660
Time(5,10)*TEOS(50,100)	1	1	1584.732	59.4354	0.0015
O2(500,700)*TEOS(50,100)	1	1	457.822	17.1706	0.0143

Scaled Estimates

Term	Scaled Estimate	Std Error	t Ratio	Prob>|t|
Intercept	117.34798	1.556894	75.37	<.0001
Time(5,10)	30.204125	1.82562	16.54	<.0001
O2(500,700)	-14.95527	1.82562	-8.19	0.0012
TEOS(50,100)	44.230975	1.82562	24.23	<.0001
Time(5,10)*O2(500,700)	-4.58305	1.82562	-2.51	0.0660
Time(5,10)*TEOS(50,100)	14.0745	1.82562	7.71	0.0015
O2(500,700)*TEOS(50,100)	-7.5649	1.82562	-4.14	0.0143

Response Standard Deviation of Oxide Thickness Across-Wafer, 9 Pts

Actual by Predicted Plot



Summary of Fit

RSquare	0.776571
RSquare Adj	**0.441428**
Root Mean Square Error	0.758641
Mean of Response	3.955355
Observations (or Sum Wgts)	11

Analysis of Variance

Source	DF	Sum of Squares	Mean Square	F Ratio
Model	6	8.001557	1.33359	2.3171
Error	4	2.302144	0.57554	Prob > F
C. Total	10	10.303701		0.2178

Lack Of Fit

Source	DF	Sum of Squares	Mean Square	F Ratio
Lack Of Fit	2	2.0224527	1.01123	7.2310
Pure Error	2	0.2796914	0.13985	Prob > F
Total Error	4	2.3021441		0.1215
				Max RSq
				0.9729

Parameter Estimates

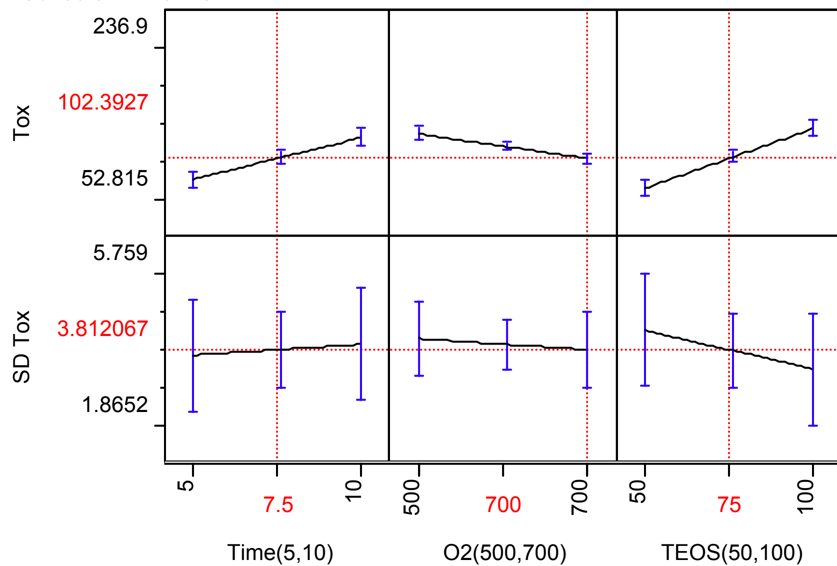
Term	Estimate	Std Error	t Ratio	Prob>|t|
Intercept	3.9553545	0.228739	17.29	<.0001
Time(5,10)	0.6834375	0.26822	2.55	0.0634
O2(500,700)	-0.143287	0.26822	-0.53	0.6215
TEOS(50,100)	-0.460187	0.26822	-1.72	0.1614
Time(5,10)*O2(500,700)	-0.543762	0.26822	-2.03	0.1126
Time(5,10)*TEOS(50,100)	-0.052262	0.26822	-0.19	0.8550
O2(500,700)*TEOS(50,100)	-0.048937	0.26822	-0.18	0.8641

Effect Tests

Source	Nparm	DF	Sum of Squares	F Ratio	Prob > F
Time(5,10)	1	1	3.7366945	6.4925	0.0634
O2(500,700)	1	1	0.1642505	0.2854	0.6215
TEOS(50,100)	1	1	1.6941803	2.9437	0.1614
Time(5,10)*O2(500,700)	1	1	2.3654213	4.1099	0.1126
Time(5,10)*TEOS(50,100)	1	1	0.0218510	0.0380	0.8550
O2(500,700)*TEOS(50,100)	1	1	0.0191590	0.0333	0.8641

Scaled Estimates

Term	Scaled Estimate	Std Error	t Ratio	Prob>|t|
Intercept	3.9553545	0.228739	17.29	<.0001
Time(5,10)	0.6834375	0.26822	2.55	0.0634
O2(500,700)	-0.143287	0.26822	-0.53	0.6215
TEOS(50,100)	-0.460187	0.26822	-1.72	0.1614
Time(5,10)*O2(500,700)	-0.543762	0.26822	-2.03	0.1126
Time(5,10)*TEOS(50,100)	-0.052262	0.26822	-0.19	0.8550
O2(500,700)*TEOS(50,100)	-0.048937	0.26822	-0.18	0.8641


Prediction Profiler
236.9
102.3927
52.815
Tox
5.759
3.812067
1.8652
SD Tox
5
7.5
10
500
700
700
50
75
100
Time(5,10)
O2(500,700)
TEOS(50,100)

Appendix C: Gen 2 Process Experiment and Analysis

E936Y Splits

E936Y Splits

Design Full Factorial

Model

Columns (4/0)

Pattern

TopTEOS

Rows

All Rows 12

Selected 0

Excluded 0

Hidden 0

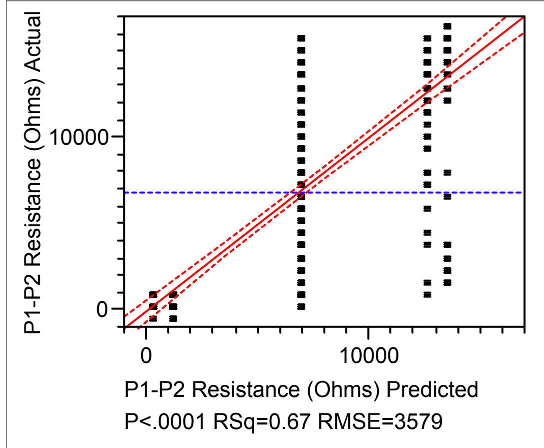
Labelled 0

	Pattern	TopTEOS	SpacerThick
1	--	3000	1000
2	++	5000	4000
3	--	3000	1000
4	-+	3000	4000
5	+-	5000	1000
6	00	4000	2500
7	00	4000	2500
8	-+	3000	4000
9	++	5000	4000
10	00	4000	2500
11	00	4000	2500
12	+-	5000	1000

Table 3: Generation 2 Process Flow Experimental Design

Response P1-P2 Resistance (Ohms)

Actual by Predicted Plot



Standard least squares analysis with an emphasis on effect screening exhibited an adjusted R^2 value of 0.67, coupled with an analysis of variance F-ratio > 492. This indicates that the variance explained by the model is 492 times greater than the variance explained by the error. The Prob>F of <0.0001 indicates that the results derived from this experiment are statistically meaningful as the probability of getting an F ratio this large if the variances of the experimental conditions were truly the same is nil. Root Mean Square Error was reported as 3579 Ω, indicating that the error in this experiment is on the order of 25% of the range of responses. Parameter estimates were investigated to optimize the model. The non-significant interaction term of the two oxide thicknesses was removed, resulting in a small R^2 increase, which simplified the analysis but did not provide a significant improvement in model accuracy.

Summary of Fit

RSquare	0.673613
RSquare Adj	0.672245
Root Mean Square Error	3579.023
Mean of Response	6846.875
Observations (or Sum Wgts)	480

Analysis of Variance

Source	DF	Sum of Squares	Mean Square	F Ratio
Model	2	1.26103e10	6.30516e9	492.2286
Error	477	6110085199	12809403	Prob > F
C. Total	479	1.87204e10		<.0001

Lack of Fit analysis produced an F-ratio of 7.79 and a Prob>F of 0.0005, with a maximum possible R^2 of 0.684. This indicates that there is significant lack of fit in the model and that the proposed model does not take into account all significant factors that affect the resistance between the Phase 1 and Phase 2 electrodes of the devices under test. This is expected, given the complexity and non-uniformity of the process, as well as variability of the measurement, although it is not desirable in general. Analysis of the residuals by predicted values and, again, by the original factors do not indicate any unaccounted for curvature in the measured response.

Lack Of Fit

Source	DF	Sum of Squares	Mean Square	F Ratio
Lack Of Fit	2	194087137	97043568	7.7917
Pure Error	475	5915998063	12454733	Prob > F
Total Error	477	6110085199		0.0005
				Max RSq
				0.6840

Parameter estimates indicate that the spacer oxide thickness and top oxide thickness are significant factors in this experiment. This agrees with basic process understanding, as thicker spacer oxide depositions should leave a thicker dielectric layer between the Phase 1 and Phase 2 electrodes, while top oxide thickness is a known effect on Phase 1 to Phase 2 resistances as determined from the Generation 1 process flow failure analysis. Effect details indicate that spacer thickness is much more significant than top oxide thickness in determining the resistance between the Phase 1 and Phase 2 electrodes.

Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Intercept	-1580.572	1037.57	-1.52	0.1283
Top Oxide (A)	-0.439012	0.211386	-2.08	0.0384

Term	Estimate	Std Error	t Ratio	Prob>|t|
Spacer Oxide (A)	4.1026647	0.137957	29.74	<.0001

Effect Tests

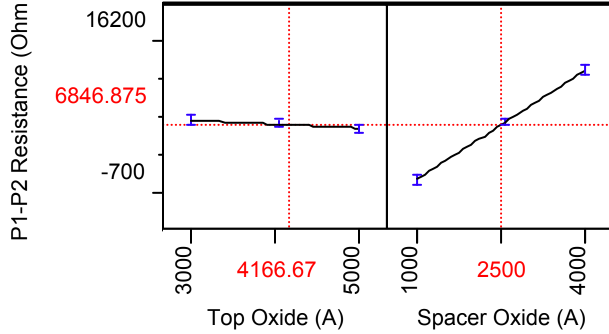
Source	Nparm	DF	Sum of Squares	F Ratio	Prob > F
Top Oxide (A)	1	1	55249613.4	4.3132	0.0384
Spacer Oxide (A)	1	1	1.13286e10	884.3950	<.0001

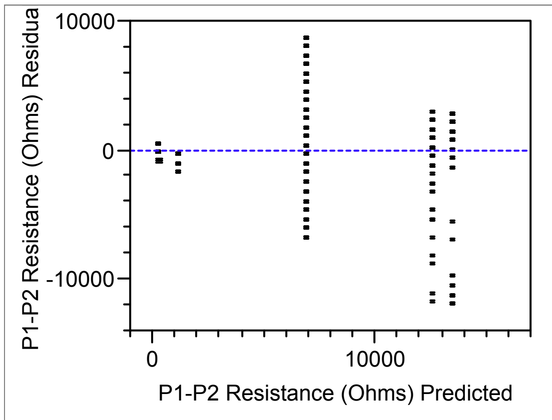
Scaled Estimates

Continuous factors centered by mean, scaled by range/2

Term	Scaled Estimate	Plot Estimate	Std Error	t Ratio	Prob>|t|
Intercept	6846.875		163.3593	41.91	<.0001
Top Oxide (A)	-439.0116		211.3858	-2.08	0.0384
Spacer Oxide (A)	6153.9971		206.9351	29.74	<.0001

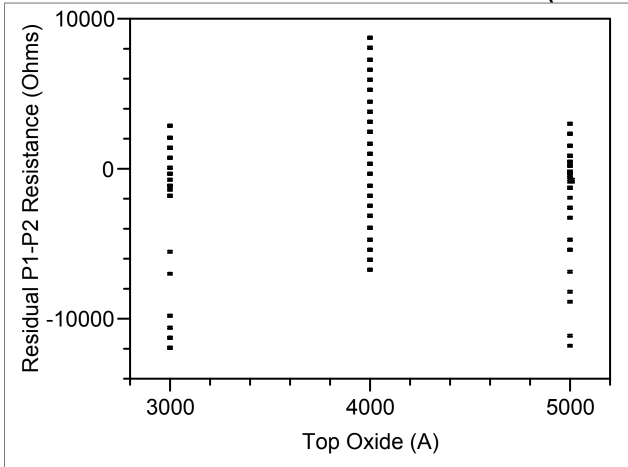
Prediction Profiler



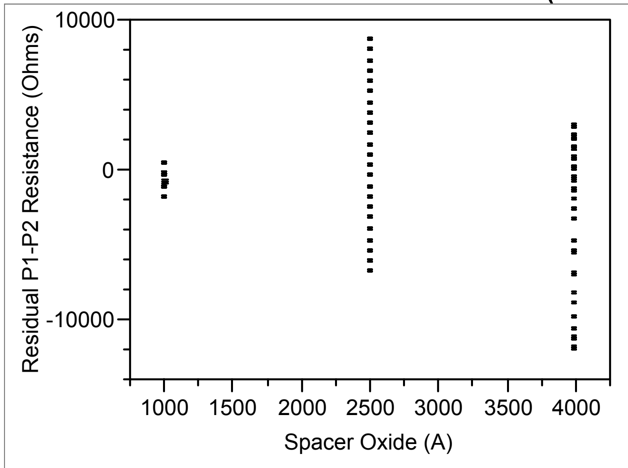


Fit Y by X Group

Bivariate Fit of Residual P1-P2 Resistance (Ohms) By Top Oxide (A)

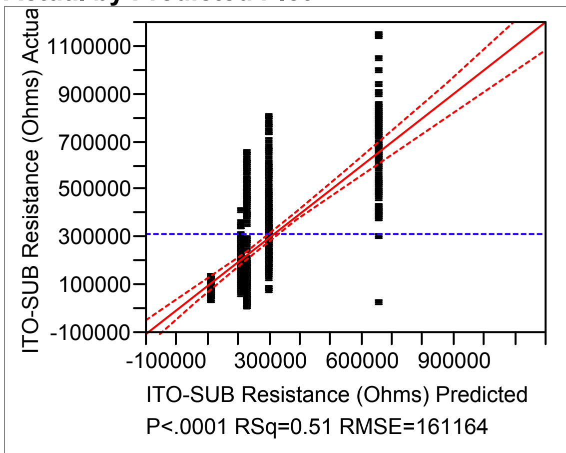


Bivariate Fit of Residual P1-P2 Resistance (Ohms) By Spacer Oxide (A)



Response ITO-SUB Resistance (Ohms)

Actual by Predicted Plot



Standard least-squares analysis with an emphasis on effect screening exhibited an adjusted R^2 value of 0.50, coupled with an analysis of variance F-ratio > 163. This indicates that the variance explained by the model is 163 times greater than the variance explained by the error. The Prob>F of <0.0001 indicates that the results derived from this experiment are statistically meaningful as the probability of getting an F ratio this

large if the variances of the experimental conditions were truly the same is nil. Root Mean Square Error was reported as 160K Ω, indicating that the error in this experiment is on the order of 15% of the range of responses. Parameter estimates were investigated to optimize the model. All parameters were found to be statistically significant, including the interaction term for the top oxide and spacer thickness.

Summary of Fit

RSquare	0.506745
RSquare Adj	0.503636
Root Mean Square Error	161163.6
Mean of Response	311119.2
Observations (or Sum Wgts)	480

Analysis of Variance

Source	DF	Sum of Squares	Mean Square	F Ratio
Model	3	1.27016e13	4.2339e12	163.0059
Error	476	1.23635e13	2.5974e10	Prob > F
C. Total	479	2.50651e13		<.0001

Lack of Fit analysis produced an F-ratio of 18.1 and a Prob>F of 0.0001, with a maximum possible R^2 of 0.525. This indicates that there is significant lack of fit in the model, and that the proposed model does not take into account all significant factors that affect the resistance between the Phase 2 electrodes and substrates of the devices under test. This is expected given the complexity and non-uniformity of the process, as well as variability of the measurement, although it is not desirable in general. Analysis of the residuals both by predicted values and again by the original factors does not indicate any unaccounted for curvature in the measured response.

Lack Of Fit

Source	DF	Sum of Squares	Mean Square	F Ratio
Lack Of Fit	1	4.5449e+11	4.5449e11	18.1277
Pure Error	475	1.1909e+13	2.5072e10	Prob > F
Total Error	476	1.23635e13		<.0001
				Max RSq
				0.5249

Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Intercept	446979.93	47407.9	9.43	<.0001
Top Oxide (A)	-81.50071	9.583725	-8.50	<.0001

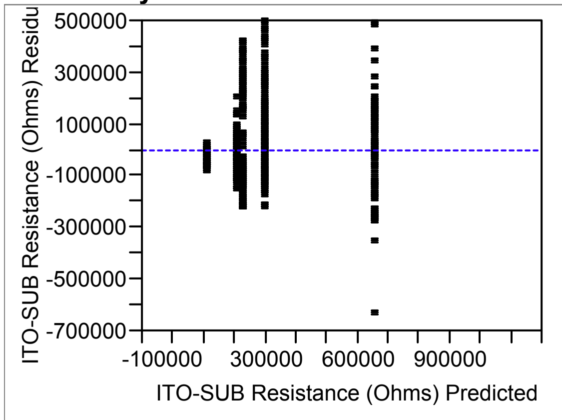
Term	Estimate	Std Error	t Ratio	Prob>|t|
Spacer Oxide (A)	72.118211	6.253573	11.53	<.0001
(Top Oxide (A)-4166.67)*(Spacer Oxide (A)-2500)	-0.09372	0.006389	-14.67	<.0001

Effect Tests

Source	Nparm	DF	Sum of Squares	F Ratio	Prob > F
Top Oxide (A)	1	1	1.8784e+12	72.3193	<.0001
Spacer Oxide (A)	1	1	3.45436e12	132.9944	<.0001
Top Oxide (A)*Spacer Oxide (A)	1	1	5.58871e12	215.1681	<.0001

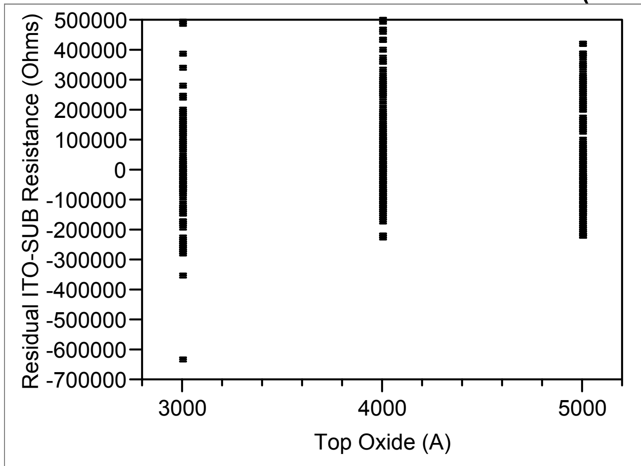
No disturbing trends were observed in analyzing the residuals by the predicted responses, not in analyzing the residuals as a function of the individual independent variables.

Residual by Predicted Plot

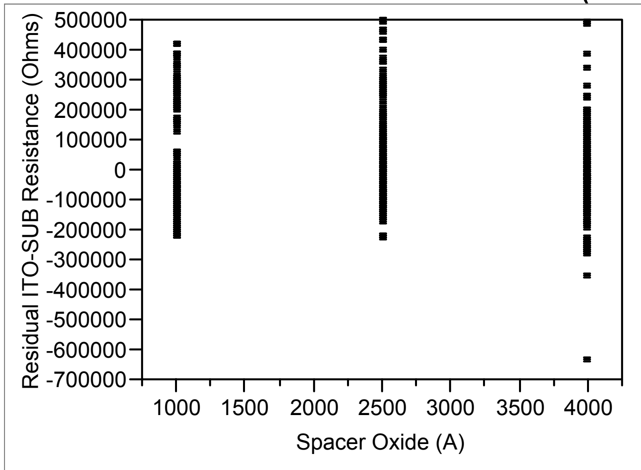


Fit Y by X Group

Bivariate Fit of Residual ITO-SUB Resistance (Ohms) By Top Oxide (A)



Bivariate Fit of Residual ITO-SUB Resistance (Ohms) By Spacer Oxide (A)



Prediction Profiler